Instituto Tecnológico de Costa Rica

Escuela de Ingeniería en Electrónica

Escuela de Ingeniería Electrónica

Sistema de adquisición de datos vía USB con aplicaciones en medición y control

Informe Final de proyecto de graduación para optar por el grado de Licenciatura en Ingeniería en Electrónica

Bismarck Álvarez Baltodano.

Cartago, septiembre de 2006

INSTITUTO TECNOLOGICO DE COSTA RICA

ESCUELA DE INGENIERIA ELECTRONICA

PROYECTO DE GRADUACIÓN

TRIBUNAL EVALUADOR

Proyecto de Graduación defendido ante el presente Tribunal Evaluador como requisito para optar por el título de Ingeniero en Electrónica con el grado académico de Licenciatura, del Instituto Tecnológico de Costa Rica.

Miembros del Tribunal

Juan Carlos Jimenez Robles	Eduardo Interiano Salguero
Profesor asesor	Profesor lector

Los miembros de este Tribunal dan fe de que el presente trabajo de graduación ha sido aprobado y cumple con las normas establecidas por la Escuela de Ingeniería Electrónica

Cartago, 20/09/06

Declaro que el presente Proyecto de Graduación ha sido realizado enteramente por mi persona, utilizando y aplicando literatura referente al tema e introduciendo conocimientos propios.

En los casos que he utilizado bibliografía he procedido a indicar las fuentes mediante la respectivas citas bibliografiítas.

En consecuencia asumo la responsabilidad total por el trabajo de graduación realizado y por el contenido del correspondiente informe final.

San José, 22 de septiembre de 2006

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Ced: 8-065-629

Dedicatoria

A mi señor Jesús, mi Dios: Por la fortaleza y la luz que me diste en los momentos mas difíciles

A mi Madre: Por que siempre fuiste un ejemplo de fortaleza, bondad y amor y por que siempre me diste tu apoyo incondicional, gracias porque se que de donde estés seguirás velando por mi. Te amo.

A mis Hermanos: Por su apoyo, confianza en mi y por llenar de aligria mi vida.

A todos aquellos que de una manera u otra me tendieron su mano para que este proyecto fuera una realidad, gracias han sido una gran bendición.

Agradecimiento:

Agradezco primeramente a mi Dios, mi señor Jesús, porque siempre me ha dado la fortaleza necesaria para salir adelante y por llenarme de bendiciones en todo momento, gracias.

De manera muy especial agradezco a mi madre, su apoyo, su amor, su empeño y su fortaleza han sido un gran ejemplo para mi vida, eres lo mas valioso que Dios me pudo haber regalado y te agradezco todo el gran esfuerzo que hiciste por mi. Te amo, gracias por todo lo que me diste.

A mis hermanos que siempre han estado con migo en los momentos difíciles, los buenos y por su gran apoyo

A los profesores que de alguna manera estuvieron involucrados con este proyecto que me tendieron la mano cuando más lo necesité.

A mis amigos que año tras año me llenan de alegría y que sin su apoyo no hubiera concluido el proyecto.

Resumen

El siguiente proyecto consiste en implementar un osciloscopio, un amperímetro y un voltímetro por medio del puerto USB de la computadora.

Como bien se sabe el osciloscopio es uno de los instrumentos más utilizados en electrónica pero su precios es muy alto y es por ello que se desea implementar un osciloscopio con ayuda del computador utilizando el puerto USB, esto con el fin de abaratar el costo de un osciloscopio para que sea más accesible incluso a los mismos estudiantes de técnico, diplomado e ingeniería en electrónica, eléctrica y cualquier área en la que se pueda utilizar un osciloscopio. Cabe mencionar que la tecnología de la computación ha avanzado a pasos agigantados abaratando los costos de las computadoras siendo más rápidas y accesibles, es por ello que se desea aprovechar aún más las capacidades de la computadora por medio de este proyecto.

Además del osciloscopio se desea que el producto también tenga la capacidad de medir corriente y tensión para extender aún más sus capacidades.

El sistema consistirá en un aparato de ¨ puntas ¨ intercambiables que se conecta al puerto USB, de tal forma de que si el usuario desea utilizar el osciloscopio le conectará al aparato una extensión que le permita utilizarlo como osciloscopio, de igual forma si desea utilizar el aparato como voltímetro solamente tendrá que conectar la extensión que le permita utilizarlo como voltímetro y de igual forma para medir corriente.

Para poder realizar este proyecto se decidió utilizar primordialmente un convertidor analógico digital y uno de los microcontroladores de la CYPRESS que incorpora puerto USB, así como amplificadores de instrumentación e integrados que proporcionan tensiónes negativas.

Abstract

The following project consists of implementing an oscilloscope, an ammeter and a voltmeter by means of port USB of the computer.

As it is known the oscilloscope is one of the used instruments more in electronics but their prices are very high and are for that reason that is desired to implement an oscilloscope with the help of the computer using port USB, this with the purpose of lowering the price of the cost of an oscilloscope so that it is more accessible even to such technician students, graduated and engineering in electronics, electrical and any area in which an oscilloscope can be used. It is possible to mention that the technology of the computation has advanced to huge steps lowering the price of the costs of the faster and accessible computers being, is for that reason that it is desired to still more take advantage of the capacities the computer by means of this project.

In addition to the oscilloscope it is desired that the product also has the capacity to measure current and tension to extend its capacities still more

The system will consist of an apparatus of ¨ interchangeable ends ¨ that is connected to port USB, of such form of that if the user wishes to use the oscilloscope he similarly connects to the apparatus an extension to him that allows him to use it like oscilloscope, if wishes to use the apparatus as voltmeter will only have to connect the extension that allows him to use it like voltmeter and similarly to measure current.

In order to be able to make this project it was decided fundamentally to use a digital analogical converter and one of the microcontrollers of the CYPRESS that incorporates port USB, as well as amplifying of instrumentation and integrated that provides negative tensions.

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Capítulo 1

1.1 Problema existente e implementación de su solución.

Los aparatos de medición en electrónica siempre se han caracterizado por ser sumamente costosos por lo que las empresas medianas y grandes, y las universidades son las únicas que pueden adquirir estos productos, no sin antes haber hecho una fuerte inversión para comprarlos, con lo que estos aparatos quedan fuera del alcance de cualquier persona que desee tener su propio laboratorio de electrónica o incluso de empresas pequeñas que necesiten adquirirlos, pero que no tengan el capital para este fin.

Actualmente en el mercado los multímetros pueden costar desde los 12000 colones hasta los 50000 colones en el país, dependiendo de las funciones que desempeñe y de su calidad. Los osciloscopios pueden tener costos que van desde los $300 hasta los $1500 dependiendo de su calidad y rango de trabajo esto en EE.UU.

Es por los costos que surge la necesidad de diseñar un aparato de medición de bajo costo y de alta calidad que pueda ser accesible y que satisfaga las necesidades de aquellos que ocupen aparatos electrónicos de medición.

1.2 Solución seleccionada

El sistema que se desea implementar es un dispositivo USB de bajo costo que permita medir corriente, tensiones y hacer las funciones de osciloscopio por tanto se decidió hacer un dispositivo de puntas intercambiables, estas puntas tendrán un valor monetario que dependerá de la función para la que fueron diseñadas y el dispositivo al que se conectarán será siempre el mismo (a este dispositivo le llamaremos dispositivo maestro y a los dispositivos que se le pueden conectar le llamaremos punta removible). Todo esto se puede observar en la figura 1.2.1 donde se muestra la primera propuesta para el diseño del embalaje. De igual manera se requirió hacer el software necesario que permita al usuario utilizar el dispositivo con la computadora.

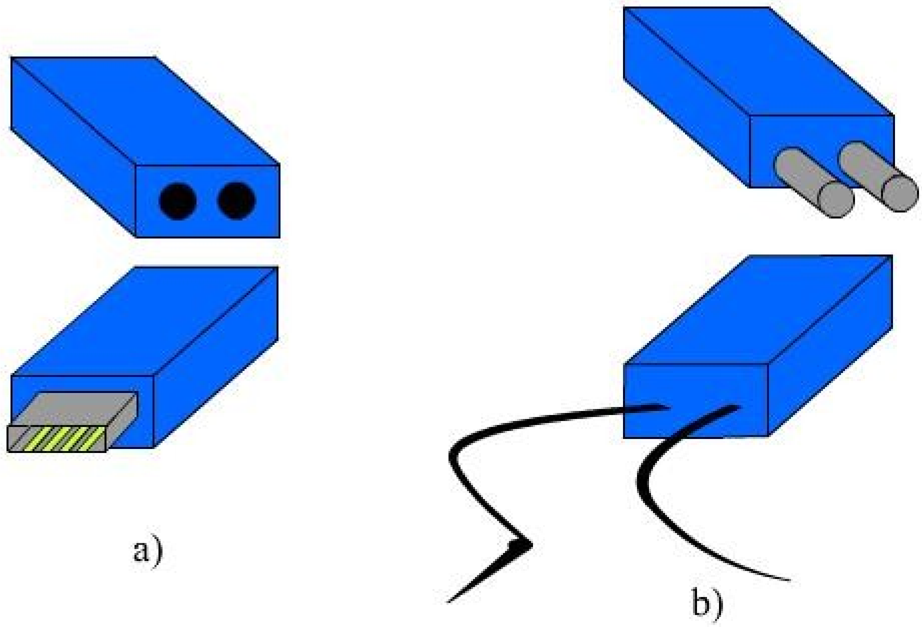


Figura 1.2.1. Dispositivo maestro y de puntas removibles.

Esto es sólo el principio de lo que realmente se podría implementar, más adelante se tiene pensado hacer puntas removibles para medir velocidad, temperatura, luminosidad y otra serie de variables físicas que puedan ser de interés no sólo para el campo de la electrónica.

Para la solución de este proyecto se decidió utilizar el microcontrolador de la CYPRESS el cy7c63001 que incorpora el puerto USB, esto debido a que ya tenia la experiencia de haber trabajado con este microcontrolador en proyectos pasados, además de ser muy económico existe suficiente información que permitió el desarrollo del proyecto sin mayor problema.

Para el dispositivo de puntas removibles se implementará con ayuda una serie de resistencias y amplificadores operacionales con un arreglo que dependerá del uso para el que sea diseñada la punta removible, además de la utilización de amplificadores de instrumentación e inversores de tensión.

Para la protección del circuito en caso de picos de corriente en la red eléctrica no se utilizó más que la protección que ya incluye la fuente de poder de la computadora.
Para la parte de programa se utilizó DELPHI que es un lenguaje de alto nivel del cual se encuentra mucha documentación y cuya base es PASCAL que fue el lenguaje con el que aprendí a programar y que me permitió la rápida comprensión de DELPHI.

Por último, en lo que respecta al embalaje del producto, debido a las dimensiones del dispositivo maestro se decidió que lo más económico seria utilizar resina para hacer el embalaje, de igual forma para las puntas removibles de amperímetro y voltímetro, pero no así para la punta de osciloscopio que por sus dimensiones ya no resulta viable utilizar resina por lo que se implementó su diseño para que sea hecho en plástico inyectado.

Capitulo 2 Meta y objetivos

2.1 Meta

Construir un producto de medición de variables físicas de bajo costo de muy buena calidad, que sea de fácil manejo para el usuario que está acostumbrado a utilizar esta clase de equipo.

2.2 Objetivos general

- Desarrollar un sistema económico que por medio del puerto USB de una PC permita medir datos de variables físicas como tensión y corriente, y además implementar un osciloscopio.

2.3 Objetivos específicos

a. Objetivos de circuiteria

- Desarrollar un dispositivo que se conecte al puerto USB de una PC, que se encargue de tomar datos analógico y convertirlos en datos digitales para que luego sean transferido a la PC por el puerto USB.
- Desarrollar los componentes (puntas removibles) que se conecten al dispositivo que va conectado a la computadora por el puerto USB (dispositivo maestro)
- Que los dispositivos sean de bajo consumo de energía de tal forma que estos puedan se alimentados con el tensión que proporciona el puerto USB.
- Implementar dispositivos que sean utilizados para medir en forma independiente corriente, tensión y permita implementar un osciloscopio, sin dañar el puerto de la PC.

b. Objetivos de programa

- Desarrollar un programa de interfaz gráfica en la computadora que permita obtener e interpretar los datos analógicos que son introducidos por los dispositivos electrónicos de tal forma que se puedan observar mediciones de corriente y tensión en la misma pantalla.
- Desarrollar un programa de interfaz gráfica en la computadora que permita obtener e interpretar los datos analógicos que son introducidos por los dispositivos electrónicos de tal forma que se pueda implementar un osciloscopio en la computadora.

c. Objetivos de documentación

- Desarrollar un manual de usuario por cada dispositivo desarrollado que facilite el uso del Programa y el circuito al usuario.

d. Objetivos de implementación

- Construir todos los circuitos como circuitos de soldadura de superficie.
- Implementar el programa de tal forma que sea amistoso para el usuario.
- Construir un embalaje que proteja los circuitos.

Capitulo 3:

3.1. Marco teórico:

Siendo que la teoría de microcontroladores, la de los convertidores analógico digital, la de voltímetros, amperímetros y osciloscopios es ya bien conocida se obviarán y se la dará prioridad a la teoría correspondiente al puerto USB.

El puerto USB nace debido a la necesidad de conectar nuevos dispositivos a una computadora sin necesidad de introducir una tarjeta controladora y que fuera de rápido acceso a diferencia de los otros puertos del PC.

USB Universal Serial Bus es una interfase plug&play entre el PC y algunos dispositivos como el teclado, el Mouse, el escáner, las impresoras, los módems, las tarjetas de sonido, las cámaras, etc.

Una característica importante es que permite a los dispositivos trabajar a velocidades que van de los 1.5 Mbps (para USB1) a los 12 Mbps (para USB 2), trabaja solamente con cuatro líneas dos de las cuales son para la transmisión y recepción de los datos, y las dos restantes son utilizadas para proporcionar energía a los dispositivos que no tengan un alto consumo y que así lo requieran proporcionando una tensión de 5v, siempre que el dispositivo no se encuentre a una distancia mayor de 5 metros.

El funcionamiento del puerto USB consiste en el paso de testigos, que es similar a otros buses como los de las redes locales en anillo con paso de testigos y la función del controlador será la de distribuir los testigos por el bus y el dispositivo que tenga la dirección igual a la portada por el testigo deberá responder enviando los datos al controlador el cual también se encarga de distribuir la energía a los dispositivos.

Utiliza una topología de estrella la cual le permite un funcionamiento simultáneo de 127 dispositivos a la vez, lo que implica la necesidad de dispositivos de tipo hub (anfitrión) que centralicen las conexiones y controlan todo el tráfico del bus. Este tipo de topología permite a diferentes dispositivos conectarse a un único bus lógico sin que los dispositivos que se encuentren más debajo de la pirámide sufran retardo.

Como se puede observar en la figura 4.1, el sistema USB consta de tres componentes el controlador, el huí y los periféricos.

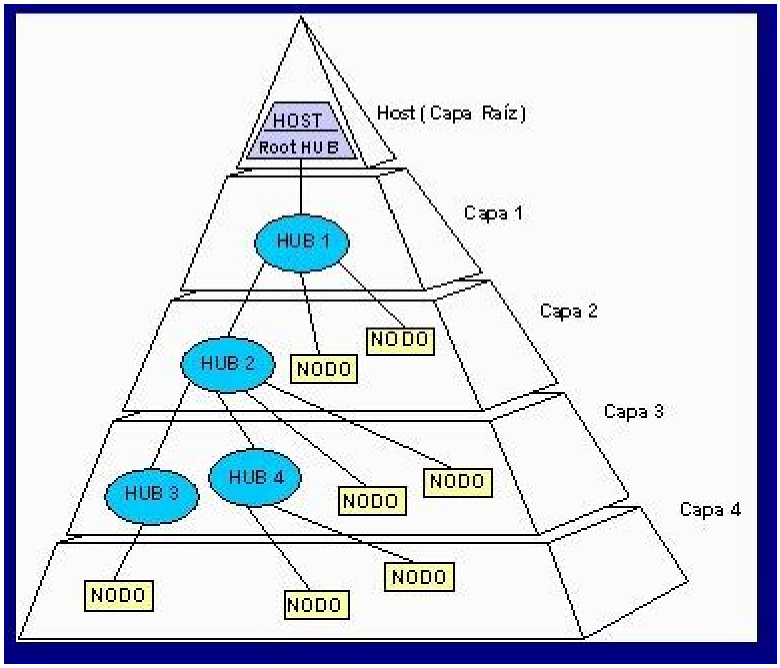


Figura 3.1.1. Estructura de capas del bus USB.

El controlador se encuentra dentro de la computadora y es el encargado de llevar a cabo la comunicación entre los dispositivos y la PC, también se encarga de estar verificando cuando se dio una conexión como una desconexión, además de que verifica que tipo de dispositivo y se encarga de asignarle una dirección lógica que utilizará cada vez que desee comunicarse con el dispositivo o viceversa. También se encarga de comunicarle al usuario si se encontró algún error en la transmisión o recepción de la información y se encarga de otorgarle los recursos necesarios del sistema al dispositivo para su adecuado funcionamiento.

La computadora también contiene el concentrador raíz el cual es quien se encarga de permitir que los datos y la energía pasen a uno o dos conectores USB del PC y de allí a los 127 periféricos que puede soportar el PC.

Con respecto a los periféricos tenemos dos clases los de baja velocidad y los de alta velocidad, en los de baja velocidad se encuentran teclados, ratones, joysticks y otros dispositivos para juegos los cuales pueden trabajar a 1.5 Mbps, con respecto a los dispositivos de alta velocidad tenemos Monitores, impresoras, scanner, módems y equipos de audio que necesitan velocidades más altas por la cantidad de volumen de información que requieren manejar estos dispositivos requieren de los 12Mbps.

En la figura 3.1.2 se muestra un diagrama de capas en el cual se puede observar como fluye la información entre las diferentes capas a nivel real y a nivel lógico.

El programa se ejecuta en el host y corresponde a un dispositivo USB (este se encuentra ya incorporado en el sistema operativo o los trae el dispositivo), hay que recordar que la conexión entre un host y un dispositivo requiere la interacción entre las capas. La capa de intertaz de bus USB proporciona la conexión física entre el host y el dispositivo. La capa de dispositivo USB es la que permite que el software del sistema USB realice operaciones genéricas USB con el dispositivo.

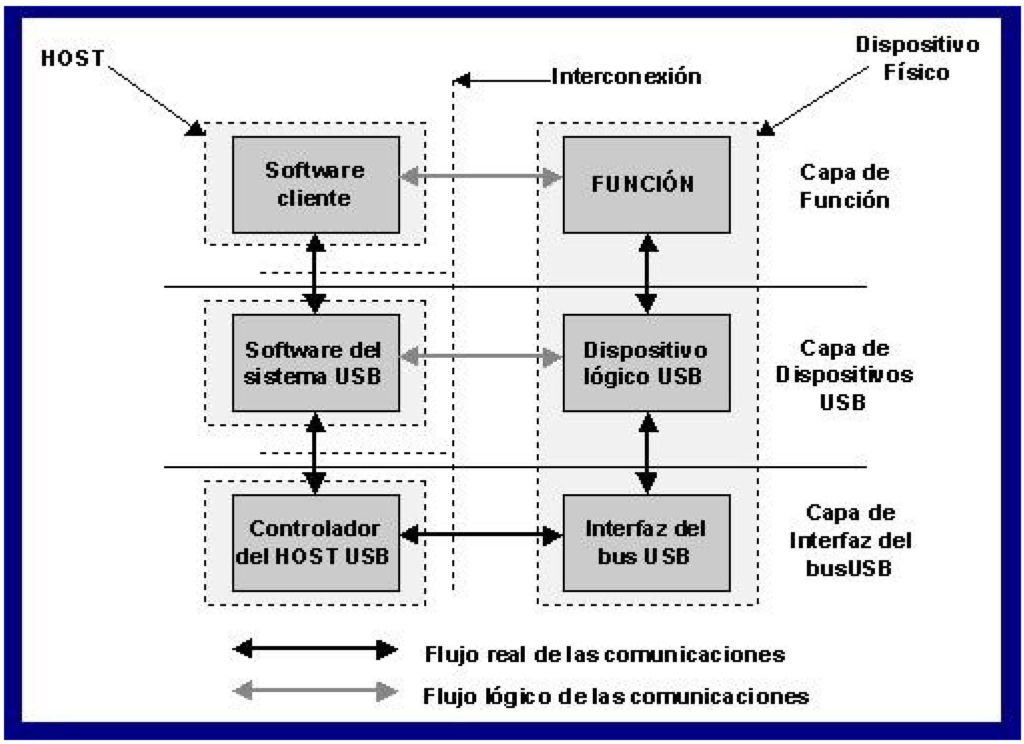


Figura 3.1.2. Capas del sistema de comunicaciones USB

La capa de función proporciona capacidades adicionales de host vía una adecuada capa de programa cliente. Las capas de función y dispositivos USB tienen cada una de ellas una visión de la comunicación lógica dentro de su nivel, aunque la comunicación entre ellas se hace realmente por la capa de interfaz de bus USB.

3.2 Descripción del sistema

Como se puede observar en la figura 3.2.1, se muestra el diagrama de bloques del dispositivo de punta removible, que es por donde se introduce la señal analógica para ser tratada antes de que esta entre al convertidor analógico digital.

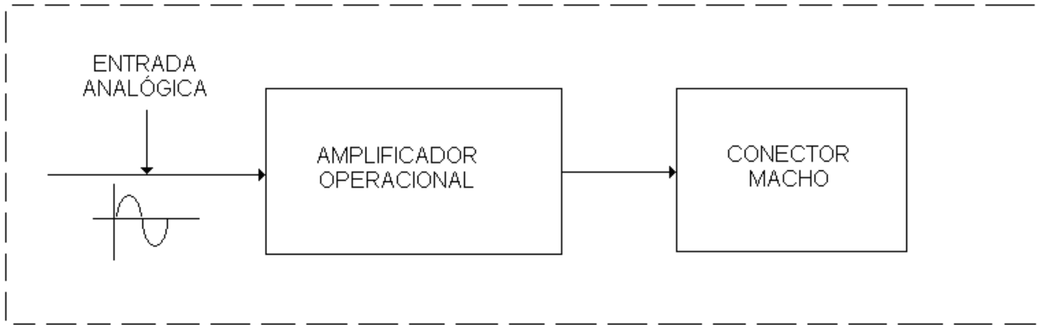


FIGURA 3.2.1. Dispositivo de punta removible.

En la figura 3.2.2, se muestra el diagrama de bloques del dispositivo maestro, el cual toma la señal analógica proveniente del dispositivo de punta removible donde se introduce en el convertidor analógico digital para luego hacer pasar los datos binarios al microcontrolador que los tomará y los sacará por el puerto USB que este incorpora, para que luego entren en la computadora donde el programa tomará los datos y los mostrará en el monitor, donde el programa a utilizar dependerá de la punta intercambiable en uso.

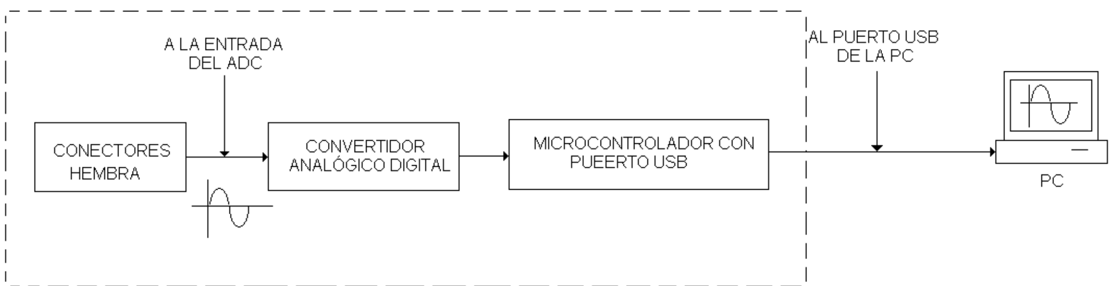


FIGURA 3.2.2. Dispositivo maestro.

El programa para el osciloscopio, voltímetro y amperímetro USB se hizo en lenguaje de alto nivel, como ya mencionó anteriormente se utilizo DELPHI 7, ya que este ambiente integrado de desarrollo (IDE) cuenta con grandes facilidades para la creación de interfaces gráficas en Windows, además de que el lenguaje Object Pascal que Delphi permite la comunicación multitarea, y de bajo nivel, con el sistema operativo de 32 bits y los puertos USB en todas sus versiones, lo que es indispensable para recolectar la señal del dispositivo de la manera más precisa. Además el código binario generado por Delphi es muy óptimo y puede ejecutarse en prácticamente cualquier versión de Windows desde la 95, sin necesidad de instalar ninguna biblioteca, ni controladores adicionales.

Unos pocos IDE, como por ejemplo Visual C++, ofrecen una velocidad de ejecución y comunicación como la que posee Delphi, pero estos IDE no cuentan con facilidades de diseño como las de Delphi, así que tomaría mucho más tiempo desarrollar la interfaz del osciloscopio que tiene una gran cantidad

de controles. Por otro lado muchos IDE, como las memorias Flash, tienen mayores facilidades para diseñar que Delphi, pero no dan libertad para comunicarse con el sistema, y la ejecución de estas aplicaciones no es para nada eficiente. Esas son las razones por las cuales se decidió utilizar Delphi/Object Pascal.

Junto al entorno Delphi se utilizó un paquete de componentes con código abierto llamado "**HIDKomponente**", que es una "envoltura" para las funciones de la biblioteca HID.DLL de Windows, lo que facilita el trabajo para la comunicación con el puerto USB siguiendo del estándar **HID** (Dispositivo de Interfaz Humana).

HID es básicamente un estándar que define un protocolo diseñado para comunicar el sistema operativo, con dispositivos de control conectados por USB como ratones, teclados y palancas de juego, pero que también permite muchas otras funciones. Las ventajas de crear un dispositivo compatible con HID es que se usa el protocolo más sencillo, y la implementación generalmente es ofrecida tanto por el fabricante del microcontrolador como por el fabricante del sistema operativo. Esto redujo muchísimo los recursos utilizados en la investigación y el desarrollo, y minimizó los errores pues se está trabajando con un estándar e implementaciones probadas ampliamente durante años. Windows reconoce, monta y desmonta dispositivos HID automáticamente sin requerir ninguna acción del usuario, y sin la necesidad de instalar software adicional. Así que los dispositivos HID tienen la característica "Plug & Play" que es un gran beneficio.

El programa entonces se encargaría principalmente de estas tareas:

3. Reconocer aquellos dispositivos USB/HID que al ser conectados se identifiquen como "**dispositivo maestro**".
4. Iniciar la comunicación con las puntas de osciloscopio, requiriendo la transmisión de los datos.
5. Obtener los datos, procesarlos y graficarlos en la interfase, según los parámetros dados por el usuario por medio de los controles.
6. Terminar o pausar la comunicación con las puntas de osciloscopio.

Algunas funciones adicionales serían:

1. Almacenar en disco la señal captada.
2. Mostrar toda la señal desde el inicio de la captura hasta el final.

La siguiente figura 3.2.3, pertenece a la interfaz implementada para el osciloscopio.

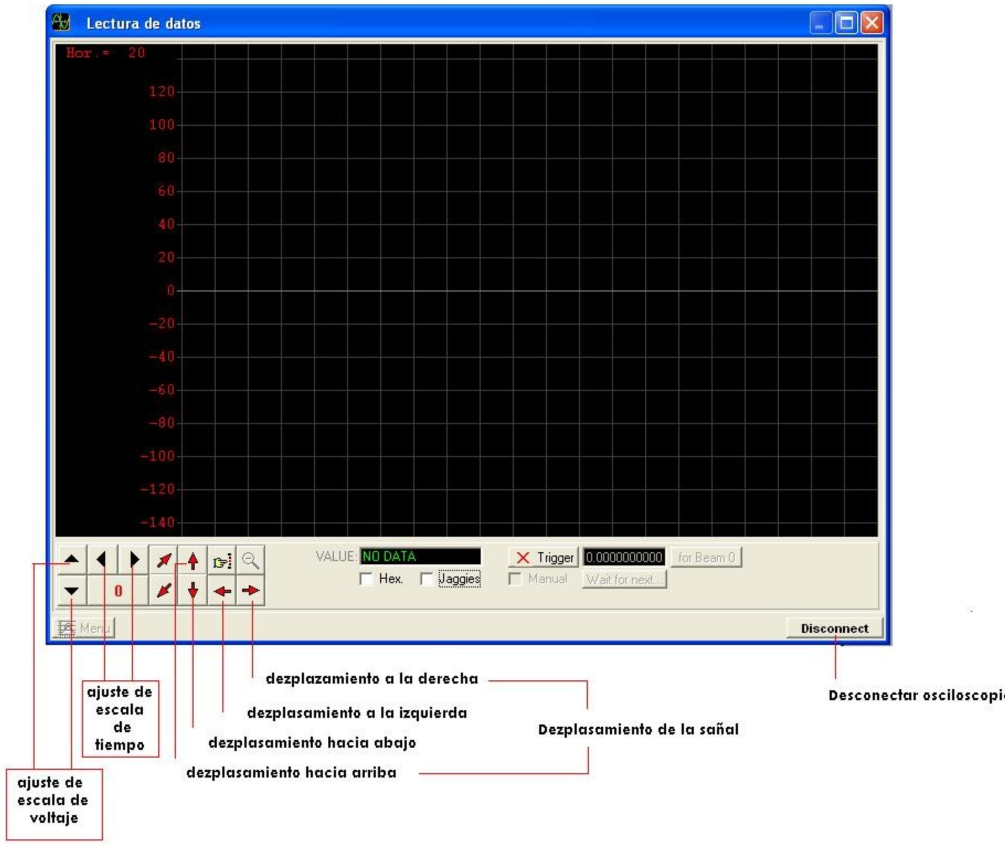


FIGURA 3.2.3 Ventana del osciloscopio.

Debido a que pueden conectarse al mismo tiempo más de una punta la cantidad de puntas que el programa pueda soportar será determinada por la capacidad de la computadora, y no por la interfaz.

Los gráficos utilizados en la interfaz no tiene un impacto importante en el consumo de recursos de la aplicación ni en su desempeño, ya que todos los elementos serán simples “fachadas” para recibir los parámetros del usuario. El único elemento que consume recursos continuamente es la representación gráfica de la onda en una pantalla virtual, ya que los datos serán procesados constantemente durante la captura de la señal.

3.3 Descripción de los principales principios Físicos, de software y/o electrónicos relacionados con la solución del problema.

Para este proyecto una de los parámetros más importantes que se tomó en cuanta es el ancho de banda de los componentes a utilizar ya que esto podía presentar una limitante para el osciloscopio pues dependiendo del ancho de banda al que trabajen los componentes electrónicos correctamente así será el ancho de banda a la que podrá trabajar el osciloscopio, por ejemplo el ancho de banda de los amplificadores a utilizar está entre 1 y los 15 MHz, el microcontrolador es de 10 MHz, aproximadamente la velocidad máxima del ADC es de 1MHz y el amplificador de instrumentación trabaja con una frecuencia de 440 MHz así que el dispositivo tendrá la máxima velocidad del componente mas lento.

También hay que tomar en cuenta la resolución a la que se desea utilizar el ADC, para nuestro caso tomaremos una resolución de 8 bits.

Los datos de corriente de entrada y de salida, así como sus respectivos voltajes fueron tomados en cuenta para todos los circuitos integrados para que haya un correcto acople entre los circuitos integrados y también el puerto USB. También se tomo en cuenta la corriente de salida del puerto USB y el voltaje que este entrega a las cargas que se le conectan para de esta forma tener claro si es posible que exista una correcta alimentación de energía por parte del puerto USB hacia los componentes electrónicos que se desean utilizar, el puerto USB puede proporcionar una corriente no mayor a 500 mA y el dispositivo que mas consume corriente es el maestro conectado con la punta de osciloscopio cuyo valor es menor a los 200 mA.

Algo muy importante que fue tomado en cuenta son los químicos a utilizar tanto para poder hacer los circuitos impresos así como el manejo de las resinas, ya que estas deben de ser utilizadas con la medida exacta de componentes, esto con el fin de evitar desperdicios, que el producto no funcione como es debido o que se produzca un accidente. Es por esto que se tomaron todas las precauciones necesarias al caso, tales como usar gabachas, anteojos de seguridad, guantes y tener los conocimientos en química necesarios para poder hacer las mezclas de la mejor forma, además del tratamiento que hay que darle a los desperdicios para que no contaminen o que contaminen lo menos posible, esto se logró depositando los residuos en ladrillos y sellándolos con cemento para que no queden expuestos al medio ambiente.

Capitulo 4 Procedimiento Metodológico del problema

4.1 Reconocimiento y definición del problema

Debido a que la tecnología USB es relativamente nueva a nivel mundial, no se ha podido encontrar ningún experto en la materia dentro del país, eso también incluye libros, es por ello que para encontrar la documentación necesaria sobre el tema se hizo una búsqueda por Internet para encontrar libros referentes al tema en otros países.

Por otro lado con respecto al uso de la resina la empresa Fibrocentro, la cual es la encargada de distribuir resina en el país también presta servicio de asesoría para sus clientes en cuanto al manejo de la resina y a la elaboración de los moldes a utilizar.

La medición de los parámetros necesarios para este proyecto tales como tiempo de reacción, ancho de banda, voltajes mínimos y máximos, etc., fueron de gran importancia para evaluar si los componentes que se desean adquirir cumplen con los requerimientos necesarios para poder desarrollar el proyecto de una forma satisfactoria.

Con respecto a la elaboración de las pistas de circuitos de montaje de superficie fueron hechas a mano debido a la carencia de un programa que pudiera hacerlas de una forma satisfactoria ya que se tuvo que combinar tanto integrados de montaje superficial como de tipo DIP.

4.2 Obtención y análisis de información

Debido a la carencia de información sobre el tema de USB en el país, como se mencionó anteriormente, se hizo uso del Internet para poder obtener información necesaria para desarrollar el sistema. Sitios de interés como amazon.com, jameco.com o digikey.com han sido fuentes importantes de información y de adquisición de componentes necesarios para este proyecto.

Con respecto a los impresos para circuitos de soldadura de superficie, existe información de cómo llevar a cabo este tipo de impresos en Internet, además como se mencionó anteriormente y con la ayuda de la Escuela de electrónica del Instituto Tecnológico que cuenta con un laboratorio de circuitos impresos y que llevaron acabo la fabricación del impreso.

Como anteriormente se mencionó la empresa Fibrocentro fue la encargada de dar la asesoría necesaria para poder hacer un embalaje con resina que permitió que el sistema a implementar sea aún más económico.

Con respecto a la circuitería necesaria para el sistema, ya la gran mayoría de los integrados han sido utilizados en uno o varios de los laboratorios cursados durante la carrera, tales como los amplificadores operacionales y el convertidos analógico digital cuyo manejo viene claramente explicado en los libros de texto utilizados en la carrera, la única diferencia fue, para el caso de los amplificadores operacionales, que se debía tomar en cuenta el ancho de banda y el voltaje de polarización ya que el circuito debe de ser de baja potencia para poder ser alimentado con la energía proveniente del puerto USB la cual es de 5 voltios y 500 mA, a esto hay que agregarle que el montaje de estos componente debe de ser, de preferencia, de superficie y también hubo que utilizar un voltaje negativo para que la señal no se recorte en su parte negativa a la hora de pasar por los amplificadores operacionales. Para encontrar los componentes que cumplieran las características anteriores se utilizaron los manuales de la Texas Instrument, Jamenco, Digi Key y los de la Nacional Semiconductors.

Con respecto al microcontrolador a utilizar este también es de montaje de superficie y al igual que el resto del circuito se alimenta con la energía del puerto USB y contener un puerto USB, para obtener un microcontrolador que se ajustara a estas necesidades se procedió a hacer una búsqueda en Internet de integrados que pudieran ajustarse a las necesidades del proyecto así que se indagó en empresas como Motorota, Texas Instruments y Microchip, pero la decisión final se tomo a favor del cy7c63001 de la empresa Cypres debido a su economía y a la cantidad de información referente a la programación del microcontrolador.

Con respecto al software implementado para poder ver en la pantalla de la computadora la información proveniente del sistema se utilizó el leguaje de programación Delphi 7 del cual existe mucha información en la biblioteca del Instituto Tecnológico, así como en la U.C.R y en Internet, a demás de que el programa facilita su manejo debido a su semejanza con el lenguaje de programación Pascal como se menciono anterior mente.

4.3 Evaluación de las alternativas y síntesis de una solución

Como ya se mencionó anteriormente lo que se requiere es implementar un sistema de bajo costo es por ello que se ha tomado la decisión de que el costo para el osciloscopio no exceda los $50 de fabricación y de que el costo para las puntas removible de corriente y voltaje no exceda el de los $5 de fabricación por pieza y de igual forma para el dispositivo maestro que no deberá exceder los $10 de fabricación, es por ello que se evaluó la utilización de los componentes necesarios, esperando que estos respondan a las necesidades requeridas. También es por esto que se desea utilizar la resina para el embalaje del circuito ya que el galón de esta no excede los 3000 colones y la resina para elaborar los moldes tiene un costo aproximado de 18000 colones y no requiere de maquinaria especializada lo cual es mucho más económico,

solamente la punta de osciloscopio que por su tamaño será necesario utilizar moldes de plástico inyectado cuyo costo esta por encima de los 400000 colones.

4.4 Implementación de la solución

Para lograr definir bien el problema y realizar una proyección certera de la posible solución es siempre necesaria una investigación exhaustiva del problema a resolver.

Para la implementación de la solución primeramente se buscó toda la información teórica necesaria para poder implementar el circuito para esto se hizo la investigación necesaria en Internet debido a que fue la fuente de información mas a mano y actualizada que se encontró.

Una vez que se obtuvo la información deseada, se procedió a hacer el estudio correspondiente.

Luego se procedió a hacer simulación en alguno de los programas para simulación de circuitos existentes para tratar de predecir de esta forma el comportamiento del circuito en la realidad.

Seleccionados todos los componentes a utilizar, se mandaron a pedir a EE.UU.

Cuando los componentes solicitados llegaron se procedió a hacer las mediciones correspondientes y a implementar los circuitos necesarios.

Con el prototipo funcionando se decidió mandar a traer los componentes de montaje de superficie para hacer los montajes correspondientes. Para esta parte los circuitos no llegaron al país así que se continuo trabajando solamente con el prototipo sin haber hecho el montaje en placas.

Se procedió a implementar el software necesario para mostrar la información en la computadora.

Ya con los circuitos y el programa realizados se procedió a hacer las mediciones y calibraciones necesarias tomando como base los voltímetros, amperímetros y osciloscopios que se encuentran en los laboratorios de electrónica.

Por último se procedió a realizar los manuales de usuarios necesarios y el informe final del proyecto.

A lo largo del proyecto, han sido necesarias algunas modificaciones de las soluciones presentadas en el siguiente capítulo, esto dado que inicialmente los

diseños electrónicos no siempre cumplen a cabalidad los objetivos y las metas de funcionamiento planteados para esa etapa en específico, así como también el circuito varia el embalaje de los circuitos también varía según las especificaciones geométricas del circuito.

4.5 Reevaluación y rediseño

Debido a que la tecnología actual en microcontroladores y en miniaturización de componentes electrónicos avanzando a pasos agigantados es recomendable estar verificando las nuevas tecnologías para de esta forma estar ofreciendo un producto de mejor calidad y más económico, además de implementar nuevas puntas intercambiables que permitan medir otras variables físicas que permitan expandir el mercado meta del producto.

Capítulo 5: Descripción detallada de la solución (Explicación del diseño)

5.1 Análisis de soluciones y selección final

Para poder llevar acabo de forma satisfactoria el adecuado funcionamiento del sistema hay que hacer un análisis de las soluciones planteadas y un estudio de las características de los materiales a utilizar para así tener la certeza de que son los mas adecuados es por ello que acontinuación se hará una descripción de cada una de las etapas de los circuitos implementados.

5.1.1 Análisis para el circuito del dispositivo maestro

Los componentes escogidos para desarrollar este circuito fueron el microcontrolador de la Cypress el cy7c63001 que ya contiene el puerto USB y como se menciono anteriormente se seleccionó este microcontrolador debido a su economía ($3.3 la unidad y $1.65 en cantidades mayores a las 100 unidades), el ADC0804 de la Nacional semiconductors ya antes utilizado en la escuela de electrónica y junto a sus 8 bit de resolución convirtió a este integrado en el más apropiado ya que también se encuentra para montaje de superficie y también a su bajo costo ($2.5 la unidad y $1.45 en cantidades mayores a las 100 unidades), el cable USB tiene un costo de $1.5, el conector mini B. USB (el puerto USB que traen las cámaras digitales) tiene un costo de $ 1 y resistencias, capacitor, cristal de 6 MHz y placa para montaje tiene un costo de $ 0.9 con lo que el costo total máximo de los materiales del dispositivo maestro es de $ 9.2

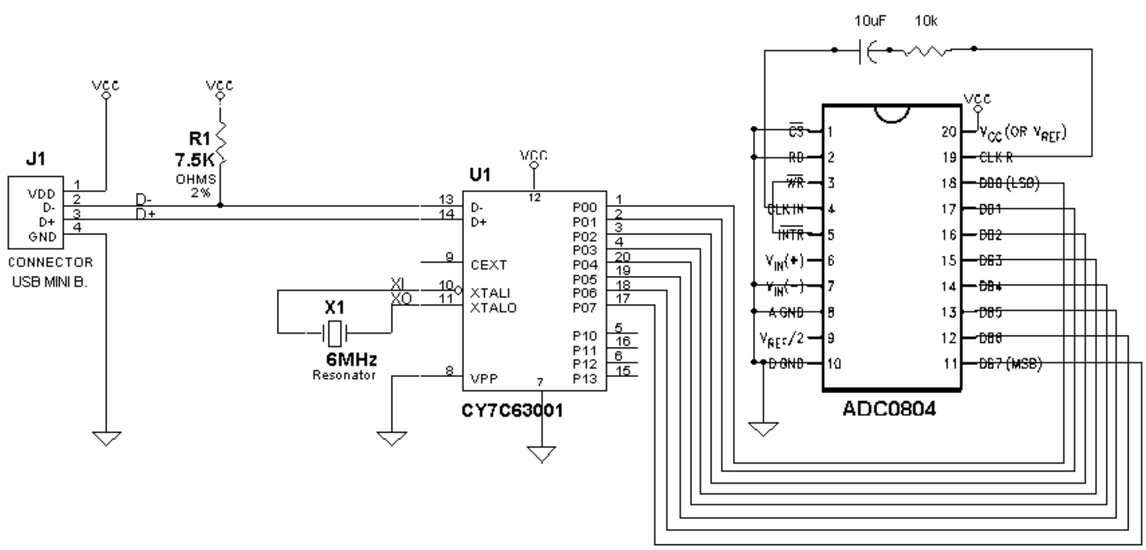


Figura 5.1.1.1 Circuito para el dispositivo maestro.

Tabla 5.1.1.1. Costo de los materiales del dispositivo maestro.

Componente	Valor por unidad ($)	Valor por unidad al adquirir mas de 100 ($)
CY7C63001	3.3	1.65
ADC0804	2.5	1.45
CABLE USB	1.5	----
MINI B. USB	1	----
CRISTAL 6MHz	0.6	----
CAPCITORES Y RESISTENCIAS	0.4	0.4
TOTAL	9.2	----

En la figura 5.1.1 se muestra el circuito del dispositivo maestro, en este se muestra que el convertidor analógico digital está con figurado para que corra libremente, esto es que esta haciendo conversiones sin necesidad de que el micro le este dando ordenes por medio de interrupciones este convertidor analógico está conectado con sus 8 bits al puerto 0 del microcontrolador cy7c63001 que es con este puerto que el microcontrolador estará tomando los datos del convertidor analógico digital para que luego con ayuda del microcontrolador que incorpora el puerto USB se puedan convertir los datos de tal forma que estos puedan ser enviados a la computador por medio del puerto USB. Como se puede observar en el ADC se encuentra una resistencia de 10 kΩ seguido de un capacitor de 150 nF con esta configuración se obtienen los pulsos de reloj necesarios para que el ADC pueda hacer sus conversiones y también determina la velocidad de las conversiones del ADC, el capacitor de 10 uF es utilizado como filtro de ruido, el voltaje de referencia del ADC es de 2.5 V este se obtiene con la ayuda de un divisor de voltaje formado por dos resistencia de 330 ohms, la resistencia de 7.5 KΩ que se encuentra entre la patilla R- y tierra del microcontrolador CY7C63001 se utiliza para decirle a la computadora que el dispositivo que se esta utilizando tiene puerto USB 1, las patillas correspondientes a R+ y R- están conectadas al puerto USB mini B. a este puerto también fueron conectados los cables de 5v y tierra para que fueran proporcionados el puerto USB de la computadora con lo que el circuito queda totalmente alimentado con el puerto USB. Este dispositivo tiene un conector hembra de 6 pines que será útil para conectar las puntas removibles, de los 6 pines se usaran 5 donde dos serán para la alimentación de energía de la punta removible, uno donde pasaran los datos analógicos hacia la entrada del ADC y por ultimo dos cables se encargaran de manejar las puntas conectadas. En la figura 5.1.1.2 se muestra el embalaje que tendría el dispositivo maestro, creado por comodidad con resina. Tomando en cuenta que el embalaje tendría un valor de $1 el dispositivo maestro tendría un valor de $9.7

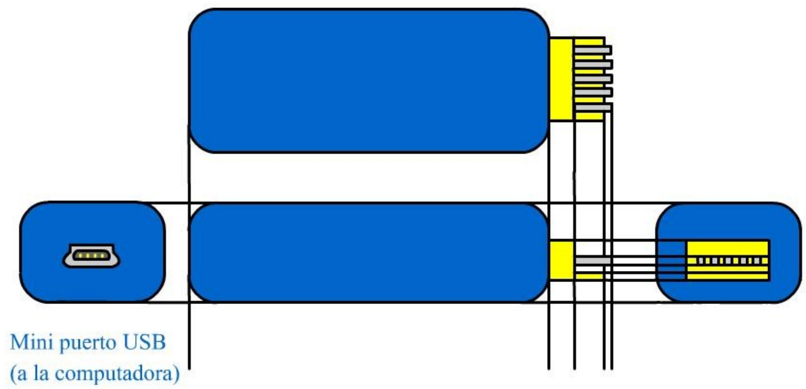


Figura 5.1.1.2. Diseño de embalaje para el dispositivo maestro.

5.1.2 Análisis para el circuito del dispositivo punta removible de voltímetro

El diseño de la punta removible de voltímetro constará simplemente de un divisor de tensión cuyo máximo valor a la entrada del dispositivo esta dada por 128 voltios y cuya menor entrada deberá de ser de 0 voltios. Este divisor de voltaje se construyó con una resistencia de 3 kΩ, una de 5 kΩ y una de 120 kΩ, permitiendo una tensión de 5 voltios para la entrada del ADC y si sacamos la relación de 128/256 nos dará el valor en el que se incrementara el voltímetro por cada cambio en los valores del ADC el cual es de 0.5 voltios el circuito se muestra en la figura 5.1.2.1. Las resistencias y la placa para el montaje del circuito tiene el valor de $0.1 el cual seria el costo total de los materiales para la contracción del circuito, el costo total de cables, conector y embalaje seria de $1, con lo que la pieza tendría el valor de $1.1

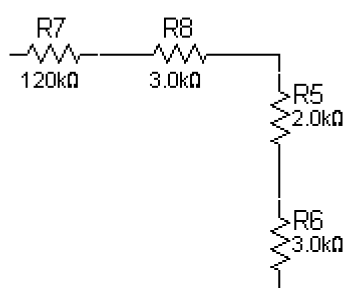


Figura 5.1.2.1. Circuito para la punta removible de voltímetro.

Y cuyo embalaje se muestra en la figura 5.1.2.2:

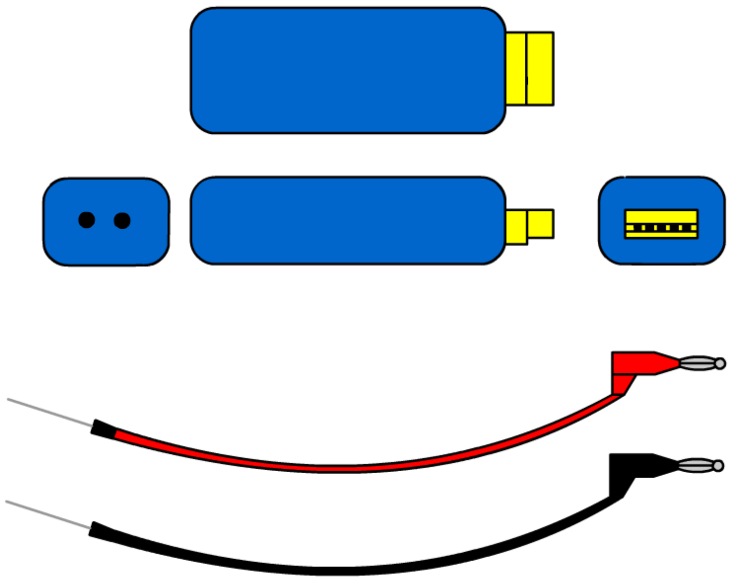


Figura 5.1.2.2. Embalaje para la punta removible de voltímetro.

Tabla 5.1.2.2. Costo de los materiales de la punta removible de voltímetro

Componentes	Valor ($)
Resistencias / Placa para montaje	0.1
Conector	0.4
Cables	0.6
TOTAL	1.1

5.1.3 Análisis para el circuito del dispositivo punta removible de amperímetro.

Como se puede observar en la figura 5.1.3.1 correspondiente al circuito del voltímetro que en la entrada de este se encuentra una resistencia de 1 ohm esta se encargara de hacer pasar la corriente a medir que será de 0 a 2.5 voltios, este valor de voltaje entrara en el amplificador operacional AD820 que la duplicara y de ahí entrará al convertidor analógico del dispositivo maestro. El valor del AD820 es de $1 y las resistencias junto con la placa para el montaje tienen un valor de $ 0.1, el costo del embalaje seria exactamente igual que el del voltímetro que es de $1 con lo que el valor total de materiales para la punta removible de amperímetro es de $2.1

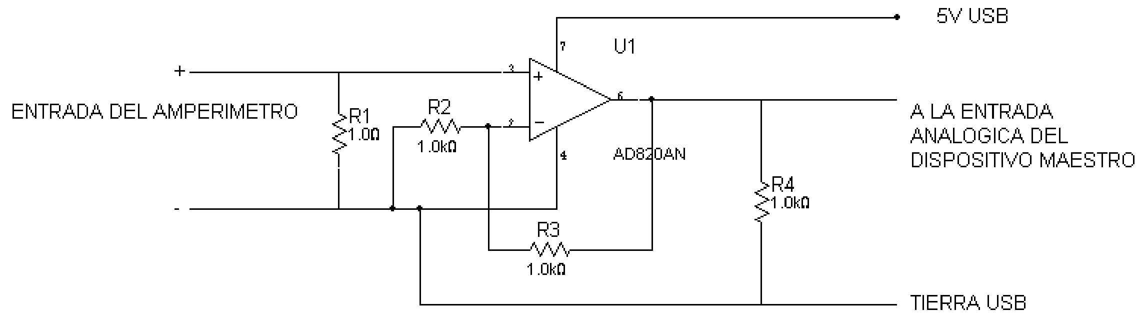


Figura 5.1.3.1. Circuito para la punta removible de amperímetro.

El embalaje de este circuito es exactamente igual que el hecho para la punta removible de voltímetro que se observa en la figura 5.1.2.2.

Tabla 5.1.3.3. Costo de los materiales de la punta removible de amperimetro

Componentes	Valor($)
AD820	1
Resistencias y Placa para montaje	0.1
Conector	0.4
Cables	0.6
TOTAL	2.1

5.1.4 Análisis para el circuito del dispositivo punta removible de osciloscopio.

En la figura 5.1.4.1. se puede observar el circuito para la punta removible de osciloscopio, el principal componente para este dispositivo fue el amplificador instrumental PGA202 de la Texas Istruments cuyo valor se encuentra por unidad en los $12.91 y mas de 100 unidades en $ 10.3, el problema con este dispositivo es que debe de trabajar con un voltaje negativo y el puerto USB no proporciona mas que un voltaje de 5 voltios positivos con lo que se tubo que agregar a la circuitería el integrado de MAXIN el MAX1673 que tiene la capacidad de invertir el voltaje de entrada, pero a este integrado se le necesita conectar una señal de reloj que sea superior en frecuencia a 1 KHz, es por eso que se introduce al circuito el famoso integrado LM555 (1 $0.92 y mas de 100 unidades $ 0.4794)el cual en configuración astable puede proporcionar los pulsos y la frecuencia necesaria para el MAX1673 (1 $5.33 y mas de 100 $2.36), con todo esto ya el PGA202 esta funcionando bien pero hay que eliminar los valores negativos de la señal de salida del PGA202 ya que hay que introducirlos en la entrada analógica del dispositivo maestro ya que este solamente trabaja con valores positivos de voltaje, es por ello que se utiliza el AD820 cuyo

valor ya se menciono antes y que tiene la habilidad de trabajar con solo una fuente de voltaje, esto permite que pueda ser utilizado para colocar la señal proveniente del PGA202 sobre un nivel de CD que permita que la señal tenga solamente valores positivos. El valor de las resistencia y los capacitares seria de aproximadamente de $2.

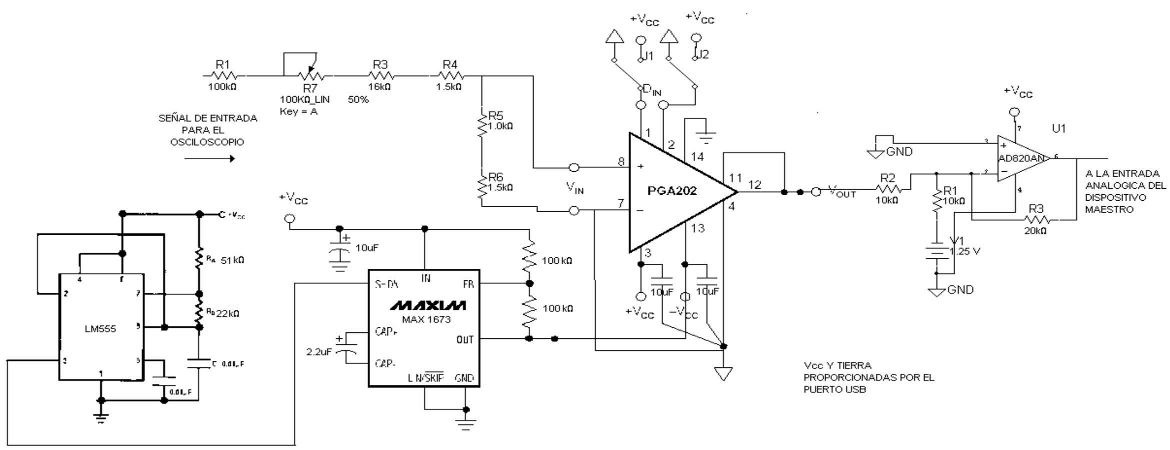


Figura 5.1.4.1. Circuito para la punta removible de osciloscopio.

El valor total para el circuito de la punta removible de osciloscopio sería de $23.26 y si a este le sumamos el embalaje que costaría $5 y el conector para el cable coaxial $1.45 el valor total seria de $18.61.

Tabla 5.1.4.4. Costo de los materiales de la punta removible de osciloscopio.

Componentes	Valor por unidad ($)	Valor por unidad al adquirir mas de 100 ($)
PGA202	12.91	10.3
MAX1673	5.33	2.36
LM555	0.92	0.4794
AD820	1	----
Conectores	1.85	----
Cables	0.6	----
Resistencias, Capacitares y Placa	2	----
TOTAL	24.61	

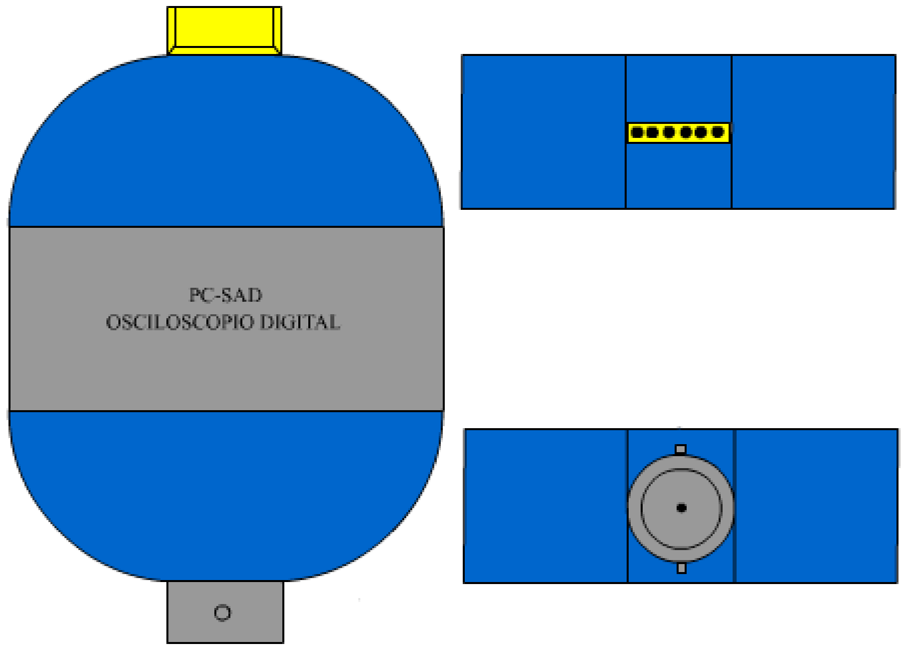


Figura 5.1.4.2. Embalaje para la punta removible de osciloscopio

5.1.5. Programa que maneja los dispositivos:

Como ya se había mencionado el dispositivo trabaja con un programa hecho en DELPHI utilizando la biblioteca gratuita para dispositivos HID y el archivo DLL para osciloscopio, este archivo DLL es el encargado de hacer que la honda se vea tal cual es en el monitor de la computadora con lo cual se ahorro mucho tiempo de programación.

En la figura siguiente se muestra la pantalla principal del programa

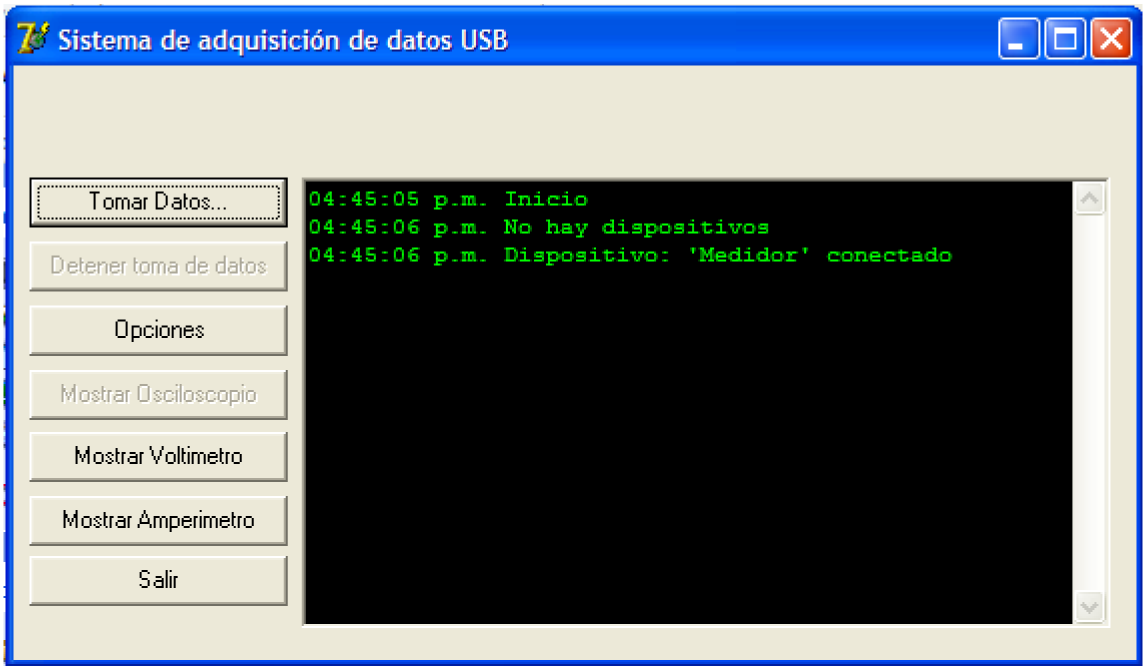


Figura 5.1.5.1. Imagen de la ventana principal del programa.

En esta ventana se muestra en una pantalla negra si el dispositivo USB esta conectado, en el botón "Tomar Datos" se debe de oprimir antes de intentar ver los datos ya sea en el osciloscopio, el voltímetro o en el amperímetro ya que con este botos se le indica a la computadora que debe de tomar todos los datos provenientes del puerto USB en uso.

Una vez oprimido el botón de "Tomar Datos" se puede oprimir el botón de "Opciones" en el cual vienen la opción de cambiar la velocidad de lectura del dispositivo USB, se puede cambiar la escala del osciloscopio o también se pueden guardar en un archivo de texto todos los datos obtenidos.

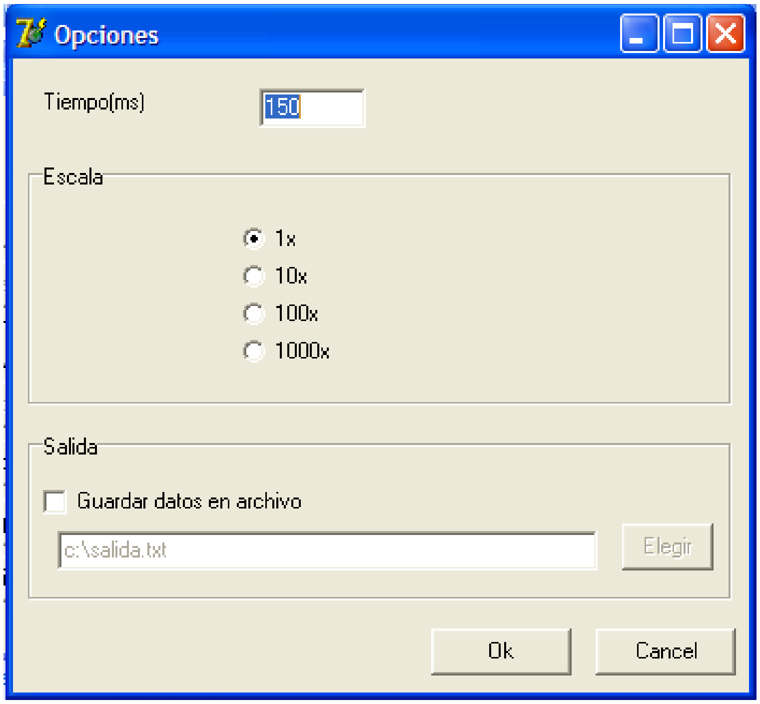


Figura 5.1.5.2. Ventana del botón de Opciones.

Ahora se puede escoger ya sea el osciloscopio, el voltímetro o el amperímetro, para escoger el osciloscopio vasta con oprimir el botón de "Mostrar Osciloscopio" y con eso aparecerá la ventana del osciloscopio donde se observarán las ondas capturadas por la computadora.

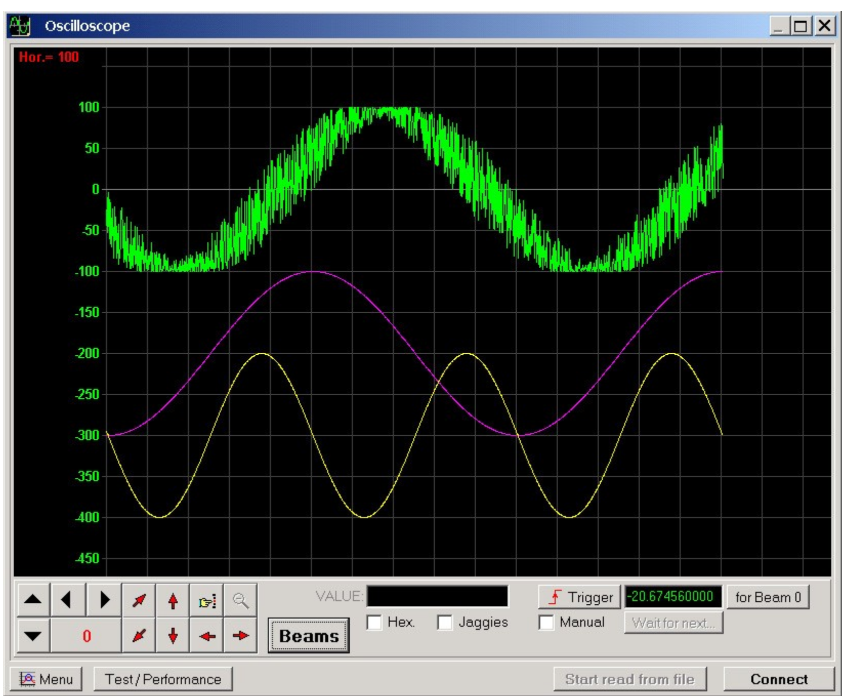


Figura 5.1.5.3. Ventana para el osciloscopio.

De igual forma para utilizar el voltímetro o amperímetro se puede oprimir los botones “Mostrar Voltímetro” o “Mostrar Amperímetro” respectivamente, con lo que aparecerán las ventanas que se muestran en las figuras 5.1.5.4 y 5.1.5.6, la ventana de voltímetro dará valores cada 0.5 voltios hasta los 128 voltios y el amperímetro dará valores cada 0.010 amperios hasta los 2.5 amperios.

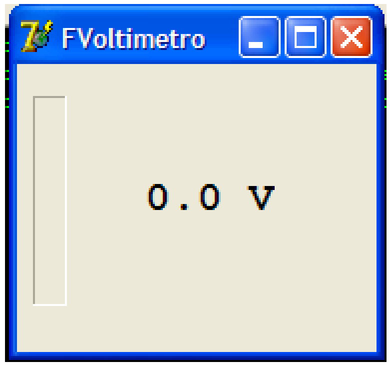


Figura 5.1.5.4. Ventana para el Voltímetro.

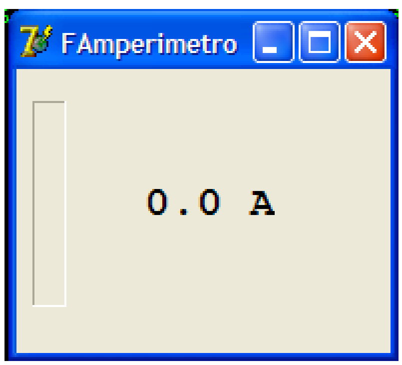


Figura 5.1.5.5. Ventana para el Amperimetro

Capítulo 6: Análisis de Resultados

Los resultados obtenidos con el dispositivo fueron muy satisfactorios ya que se calibraron con ayuda de instrumentos de medición de los laboratorios de electrónica y las mediciones realizadas con los dispositivos dieron valores idénticos a los valores obtenidos con los instrumentos de medición de la escuela de electrónica.

A continuación se mostrarán varias imágenes de fotos tomadas entre los instrumentos de medición del laboratorio de electrónica y los dispositivos de medición implementados para este proyecto.

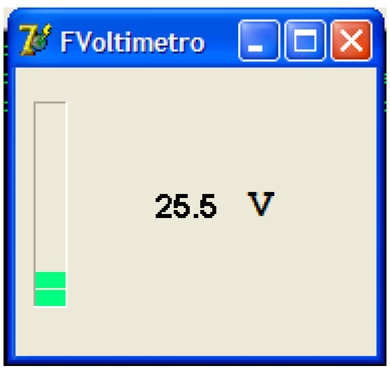




Figura 6.1. Imagen que muestra la medición de tensión bajo iguales condiciones entre el programa y un multímetro

Como se puede observar en las dos imágenes presentadas en la figura 6.1. utilizando un circuito de prueba para hacer las mediciones de tensión ambas mediciones son idénticas.

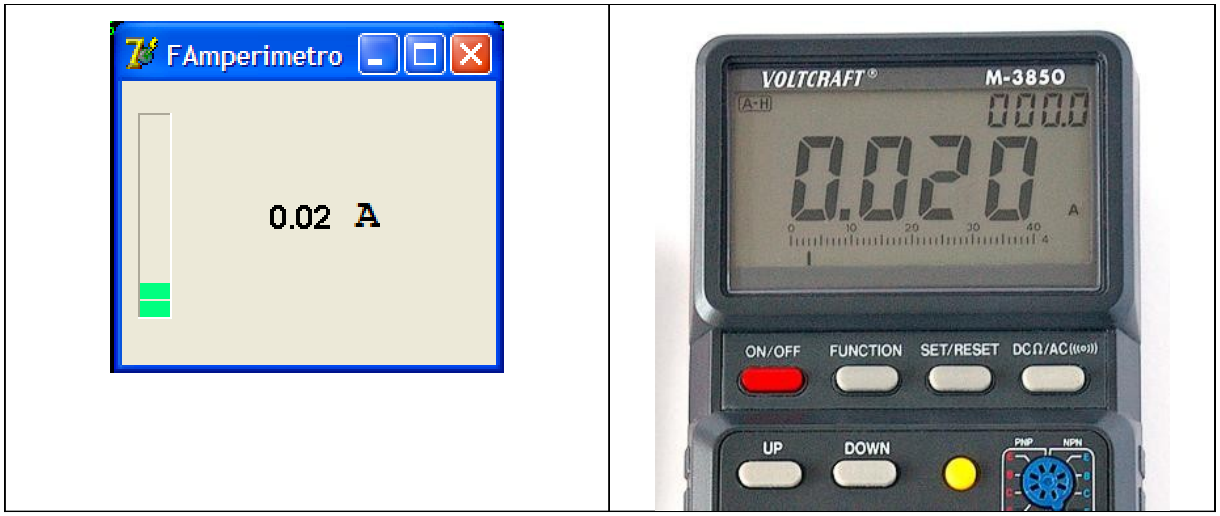


Figura 6.2. Imagen que muestra las mediciones de corriente a iguales condiciones entre el programa y un multímetro.

Como se puede observar nuevamente bajo las mismas condiciones de medición, esto es utilizando un circuito de prueba para hacer las mediciones, el dispositivo de punta removible de amperímetro esta dando exactamente la misma medición que el multímetro digital.

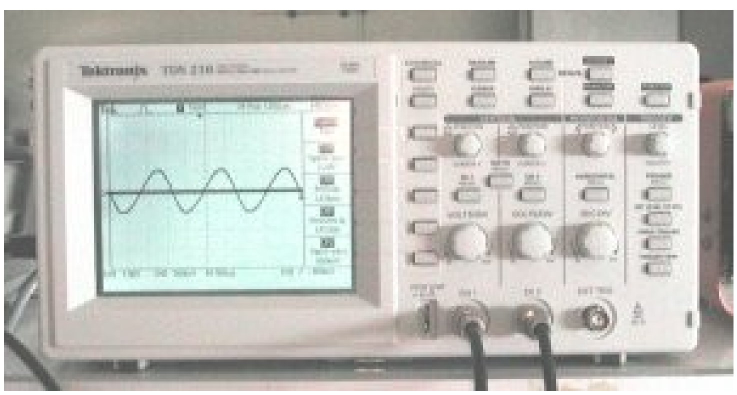


Figura 6.3. Imagen que muestra una medición hecha con el osciloscopio del laboratorio de la escuela de electrónica.

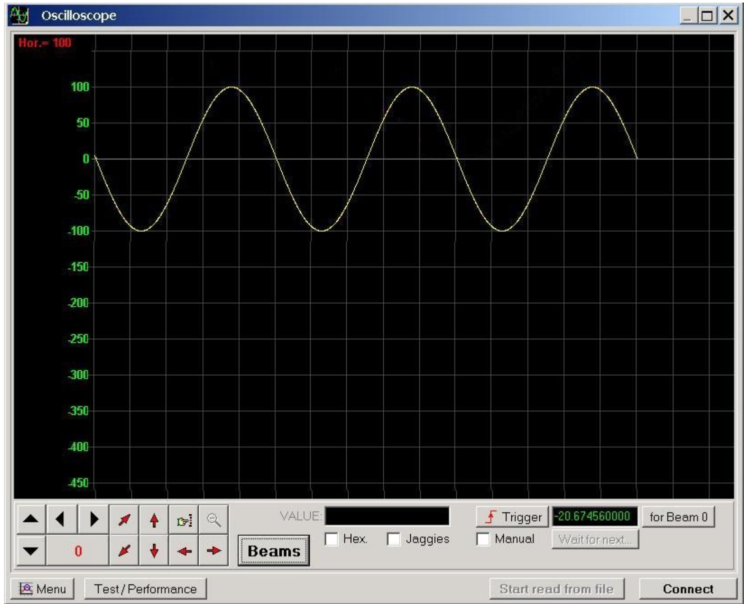


Figura 6.4. Imagen que muestra una medición hecha con el dispositivo de punta removible del osciloscopio.

Como se puede observar en la figura 6.3. y la figura 6.4. las mediciones de la onda son idénticas, esto debido a que se utilizó el mismo circuito de prueba para ambos dispositivos de medición.

Estas mediciones han demostrado que el dispositivo de adquisición de datos implementado por USB es totalmente funcional, satisfaciendo los objetivos esperados.

Tabla 6. Características eléctricas de la punta de osciloscopio

Parámetros	Sin dispositivo maestro	Con dispositivo maestro
Voltaje de alimentación	5 V	5 V
Voltaje de entrada	220 Vp	220 Vp
Corriente de alimentación	49.9 mA	53.6 mA
Corriente de entrada	50 pA	50 pA
Impedancia de entrada	10 GΩ	10 GΩ
Respuesta de frecuencia	1 MHz	6 Hz

Capítulo 7:

7.1 Conclusiones

1. La utilización de integrados inversores de potencial reduce la circuitería y proporciona la tensión necesaria para los amplificadores de instrumentación.
2. Con los amplificadores de instrumentación se evita el uso de multiplexores analógicos, se economiza espacio y tiempo a la hora de construir el ciruito.
3. Con la ayuda de un integrado que trabaje con una fuente de tensión positivo se puede lograr introducir un nivel de offset a una señal analógica permitiendo que esta señal sea luego introducida a un ADC sin que su forma se vea alterada.
4. Con la ayuda de los microcontroladores se puede implementar la comunicación entre un dispositivo y la PC.
5. El puerto USB de la computadora permite introducir datos analógicos en forma de Bits a la PC para que esta pueda representar estos datos en el monitor.
6. No todos los integrados es posible encontrarlos para que sean de montaje de superficie.

7.2 Recomendaciones

1. Para ampliar el ancho de banda bajo el cual trabaja el dispositivo de adquisición de tatos por USB no hay que usar el PGA202 si no que se implementa su misma función con amplificadores operacionales y multiplexores analógicos.
2. Cambiar el ADC0804 por un convertidor de mayor velocidad.
3. Se pueden utilizar integrados equivalentes a los que se utilizaron en este proyecto para reducir el costo por materiales.
4. Para que las pistas en un circuito impreso queden de mayor calidad el circuito debe de tener la mayor cantidad de cobre posible.
5. Se puede utilizar el microcontrolador de la microchip el 16c745 con lo que se reduciría el costo de fabricación y de materiales del dispositivo maestro.

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3. **Cypress, CY7C63001 <u>Datasheet.</u>**

Internet:

http://www.tutorialesenlared.com/index.php?sid=922051542&t=sub_pages&cat=3

http://es.wikipedia.org/wiki/Microcontrolador

http://www.monografias.com/trabajos13/fire/fire.shtml

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http://www.oscilloscope-lib.com

APENDICE.

Glosario:

- USB (universal serial bus): bus serial universal, puerto de comunicaciones serial de alta velocidad que utiliza solamente dos hilos para entablar comunicación entre un dispositivo y la computadora.

- Testigos (tokens): el controlador USB utiliza los testigos que son códigos que contienen las direcciones de los dispositivos conectados al puerto.

- Tramas: tiempo utilizado entre la comunicación a través de transacciones.

- Transacciones: información compuesta por testigos (tokens), Datos y validación (Handshake)

- Validación: Bandera que se utiliza para indicar el resultado de la Transacción

- Bulk: Tipo de transferencia de datos de grandes cantidades.

- Isócrono: Tipo de transferencia de datos de gran ancho de banda utilizado para audio, telefonía y video.

- USB 1.0: Protocolo USB cuya velocidad máxima de transmisión es de 1.5 Mbps

- HID (human interface device): dispositivo de interfaz humana, es un protocolo de comunicación USB utilizado para ciertos dispositivos.

- Dll (Dynamic Link Library): "Biblioteca de vínculos dinámicos" es un archivo que contiene funciones que se pueden llamar desde aplicaciones u otras Dll. Los desarrolladores utilizan las Dll para poder reciclar el código y aislar las diferentes tareas. Las Dll no pueden ejecutarse directamente, es necesario llamarlas desde un código externo.

CY7C63000
CY7C63001
CY7C63100
CY7C63101
CY7C63200
CY7C63201
Universal Serial Bus Microcontroller

Cypress Semiconductor Corporation • 3901 North First Street • San Jose • CA 95134 • 408-943-2600
October 1996 - Revised June 26, 1997

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- **USB Specification Compliance**
  - **— Conforms to USB 1.5 Mbps Specification, Version 1.0**
  - **— Conforms to USB HID Specification, Version 1.0**
  - **— Supports 1 device address and 2 endpoints**
- **8-bit RISC microcontroller**
  - **— Harvard architecture**
  - **— 6 MHz external ceramic resonator or clock crystal**
  - **— 12 MHz internal operation**
  - **— USB optimized instruction set**
- **Internal memory**
  - **— 128 bytes of RAM**
  - **— 2K bytes of EPROM (CY7C63000, CY7C63100, CY7C63200)**
  - **— 4K bytes of EPROM (CY7C63001, CY7C63101, CY7C63201)**
- **I/O ports**
  - **— Integrated USB transceivers**
  - **— Up to 16 Schmitt trigger I/O pins with internal pull-up**
  - **— Up to 8 I/O pins with LED drive capability**
  - **— Special purpose I/O mode supports optimization of photo transistor and LED in mouse application**
  - **— Maskable Interrupts on all I/O pins**
- **8-bit free-running timer**
- **Watchdog timer (WDT)**
- **Internal power-on reset (POR)**
- **Improved output drivers to reduce EMI**
- **Operating voltage from 4.0V to 5.25VDC**
- **Operating temperature from 0 to 70 degree Celsius**
- **Available in space saving and low cost 18-pin PDIP, 20-pin PDIP, 20-pin SOIC, and 24-pin SOIC packages**
- **Windowed packages also available to support program development: 18, 20, and 24-pin Windowed CerDIP**
- **Industry standard programmer support**

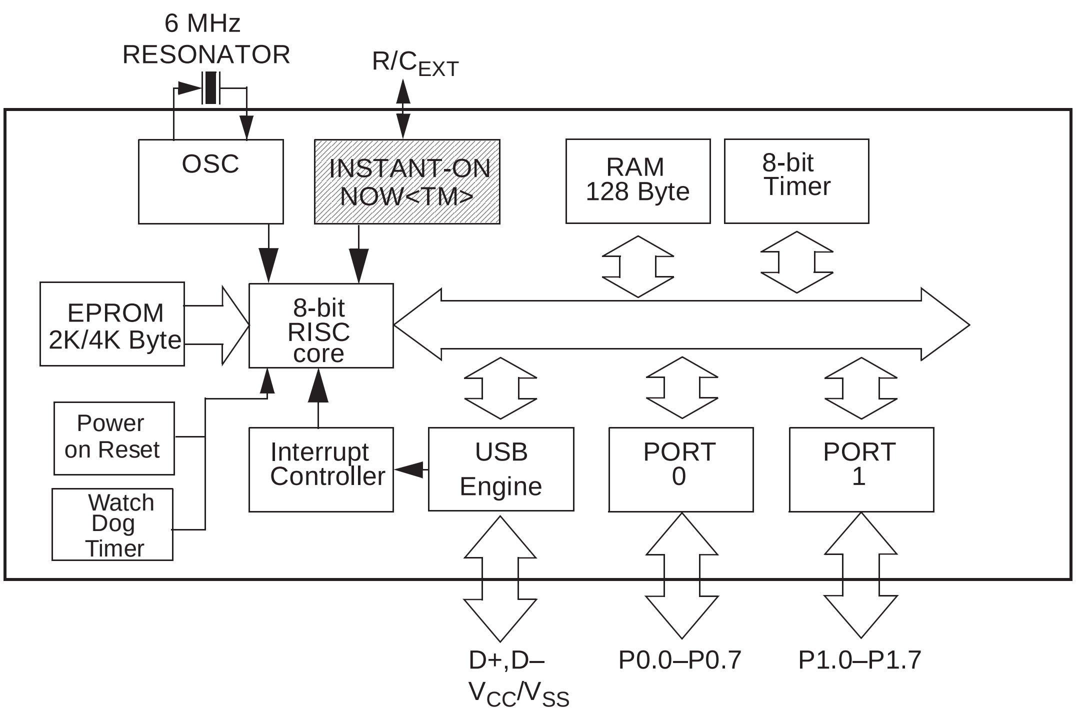
2.0 Functional Overview

The CY7C63xxx is a family of 8-bit RISC One Time Programmable (OTP) microcontrollers with a built-in 1.5-Mbps USB serial interface engine. The microcontroller features 35 instructions which are optimized for USB applications. There is 128 bytes of onboard RAM available incorporated into each microcontroller. The Cypress USB Controller accepts a 6 MHz ceramic resonator or a 6 MHz crystal as its clock source. This clock is doubled within the chip to provide a 12 MHz clock for the microprocessor.

The microcontroller features two ports of up to sixteen general purpose I/Os (GPIOs). Each GPIO pin can be used to generate an interrupt to the microcontroller. Additionally, all pins in Port 1 are equipped with programmable drivers strong enough to drive LEDs. The GPIO ports feature low EMI emissions as a result of controlled rise and fall times, and unique output driver circuits in the microcontroller. The Cypress microcontrolles have a range of GPIOs to fit various applications; the CY7C630xx has twelve GPIO, the CY7C631xx has sixteen GPIO, and the CY7C632xx has ten GPIO. Notice that each part has eight ‘low-current’ ports (Port 0)with the remaining ports (Port 1) being ‘high-current’

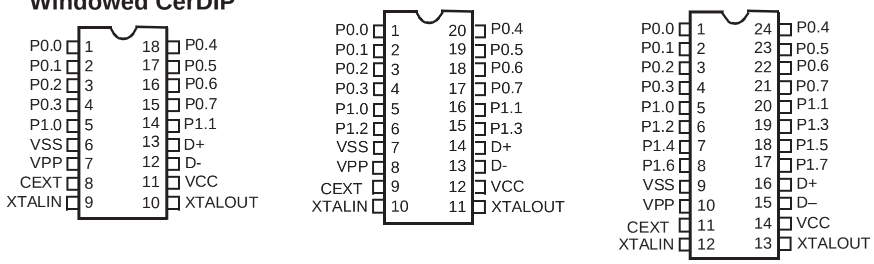
The twelve GPIO CY7C6300x is available in is a 20-pin PDIP (-PC), 20-pin SOIC (-SC), and a 20-pin Windowed CerDIP. The sixteen GPIO CY7C6310x is available in a 24-pin SOIC (-SC) and a 24-pin Windowed CerDIP (-SC). The ten GPIO CY7C6320x is available in an 18-pin PDIP (-PC) and an 18-pin Windowed CerDIP (-WC).

Logic Block Diagram



Pin Configurations (Top View)

18-pin DIP/ Windowed CerDIP — **20-pin DIP/SOIC/ Windowed CerDIP** — **24-pin SOIC/ Windowed CerDIP**



6311–1

3.0 Pin Definitions

Name	I/O	18-Pin	20-Pin	24-pin	Description
P0.0	I/O	1	1	1	Port 0 bit 0
P0.1	I/O	2	2	2	Port 0 bit 1
P0.2	I/O	3	3	3	Port 0 bit 2
P0.3	I/O	4	4	4	Port 0 bit 3
P0.4	I/O	18	20	24	Port 0 bit 4
P0.5	I/O	17	19	23	Port 0 bit 5
P0.6	I/O	16	18	22	Port 0 bit 6
P0.7	I/O	15	17	21	Port 0 bit 7
P1.0	I/O	5	5	5	Port 1 bit 0
P1.1	I/O	14	16	20	Port 1 bit 1
P1.2	I/O	–	6	6	Port 1 bit 2
P1.3	I/O	–	15	19	Port 1 bit 3
P1.4	I/O	–	–	7	Port 1 bit 4
P1.5	I/O	–	–	18	Port 1 bit 5
P1.6	I/O	–	–	8	Port 1 bit 6
P1.7	I/O	–	–	17	Port 1 bit 7
XTALIN	I	9	10	12	Crystal / Ceramic resonator in or external clock input
XTALOUT	O	10	11	13	Crystal / Ceramic resonator out
CEXT	I/O	8	9	11	Connects to external R/C timing circuit for optional suspend wakeup
D+	I/O	13	14	16	USB data+
D–	I/O	12	13	15	USB data–
VPP	–	7	8	10	Programming voltage supply, tie to ground during normal operation
V_{CC}	–	11	12	14	Voltage supply
V_{SS}	–	6	7	9	Ground

4.0 Pin Description

Name	Description
V_{DD}	1 pin. Connects to the USB power source or to a nominal 5V power supply. Actual V_{CC} range can vary between 4.0V and 5.25V
V_{SS}	1 pin. Connects to ground
V_{PP}	1 pin. Used in programming the on-chip EPROM. This pin should be tied to ground during normal operations.
XTALIN	1 pin. Input from an external ceramic resonator, crystal, or clock
XTALOUT	1 pin. Return path for the ceramic resonator or crystal
P0.0–P0.7, P1.0–P1.7	16 pins. P0.0–P0.7 are the 8 I/O lines in Port 0. P1.0–P1.7 are the 8 I/O lines in Port 1. Please note that P1.0–P1.1 are supported in the CY7C6320x and P1.0–P1.3 are supported in the CY7C6300x. All I/O pins are pulled up internally by 16KΩ resistors. However, the sink current of each pin can be programmed to one of sixteen levels. Besides functioning as general purpose I/O lines, each pin can be programmed as an interrupt input. The interrupt is edge-triggered, with programmable polarity.
D+, D–	2 pins. Open-drain I/O with 2 pins. Bidirectional USB data lines. An external 7.5 KΩ resistor must be connected between the D– pin and V_{CC} to select low-speed USB operation.
CEXT	1 pin. Open-drain output with Schmitt trigger input. The input is connected to a level-sensitive (HIGH) interrupt. CEXT may be connected to an external RC to generate a wake-up from Suspend mode. See Section 5.6.

5.0 Functional Description

The Cypress CY7C63000/1, CY7C63100/1, and CY7C63200/1 USB microcontrollers are optimized for human-interface computer peripherals such as a mouse, joystick, and gamepad. Cypress USB microcontrollers conform to the low-speed (1.5 Mbps) requirements of the USB Specification version 1.0. Each micorcontroller is a self-contained unit with a USB interface engine, USB transceivers, an 8-bit RISC microcontroller, a clock oscillator, timers, and program memories. It supports one USB device address and two end points.

The 6 MHz clock generated by the on-chip oscillator is stepped up to 12 MHz to drive the microcontroller. A RISC architecture with 35 instructions is chosen to provide the best balance between performance and product cost.

5.1 Memory Organization

The memory in the USB Controller is organized into user program memory in EPROM space and data memory in SRAM space.

5.1.1 Program Memory Organization

The 14-bit Program Counter (PC) is capable of addressing 16K bytes of program space. However, the program space of the CY7C63000, CY7C63100 and CY7C63200 is 2K bytes. For applications requiring more program space, the CY7C63001, CY7C63101 and CY7C63201 each offer 4K bytes of EPROM. The program memory space is divided into two functional groups: Interrupt Vectors and program code.

The interrupt vectors occupy the first 16 bytes of the program space. Each vector is 2 bytes long. After a reset, the Program Counter points to location zero of the program space. *Figure 5-1* shows the organization of the Program memory Space.

5.1.2 Security Fuse Bit

The Cypress USB microcontroller includes a security fuse bit. When the security fuse is programmed, the EPROM program memory outputs 0xFF to the EPROM programmer, thus protecting the user’s code.

after reset: PC → 0x0000

Address	
0x0000	Reset Vector
0x0002	Interrupt Vector - 128 µs
0x0004	Interrupt Vector - 1.024 ms
0x0006	Interrupt Vector - USB Endpoint 0
0x0008	Interrupt Vector - USB Endpoint 1
0x000A	Reserved
0x000C	Interrupt Vector - GPIO
0x000E	Interrupt Vector - Cext
0x0010	On-chip program Memory
0x07FF	2K ROM (CY7C63000, CY7C63100,CY7C63200)
0x0FFF	4K ROM (CY7C63001, CY7C63101, CY7C63201)

Figure 5-1. Program Memory Space

5.1.3 Data Memory Organization

The USB Controller includes 128 bytes of data RAM. The upper 16 bytes of the data memory are used as USB FIFOs for End Point 0 and End Point 1. Each end point is associated with an 8-byte FIFO.

The USB controller includes two pointers into data RAM, the Program Stack Pointer (PSP) and the Data Stack Pointer (DSP). The value of PSP after reset is 0x00. The PSP is incremented by 2 whenever a CALL instruction is executed and it is decremented by 2 whenever a RET instruction is used.

The DSP is pre-decremented by 1 whenever a PUSH instruction is executed and it is incremented by 1 after a POP instruction is used. The default value of the DSP after reset is 0x00, which would cause the first PUSH to write into USB FIFO space for End Point 1. Therefore, the DSP should be mapped to a location such as 0x70 before initiating any data stack operations. Refer to the Reset section for more information about DSP re-mapping after reset. *Figure 5-2* illustrates the Data Memory Space.

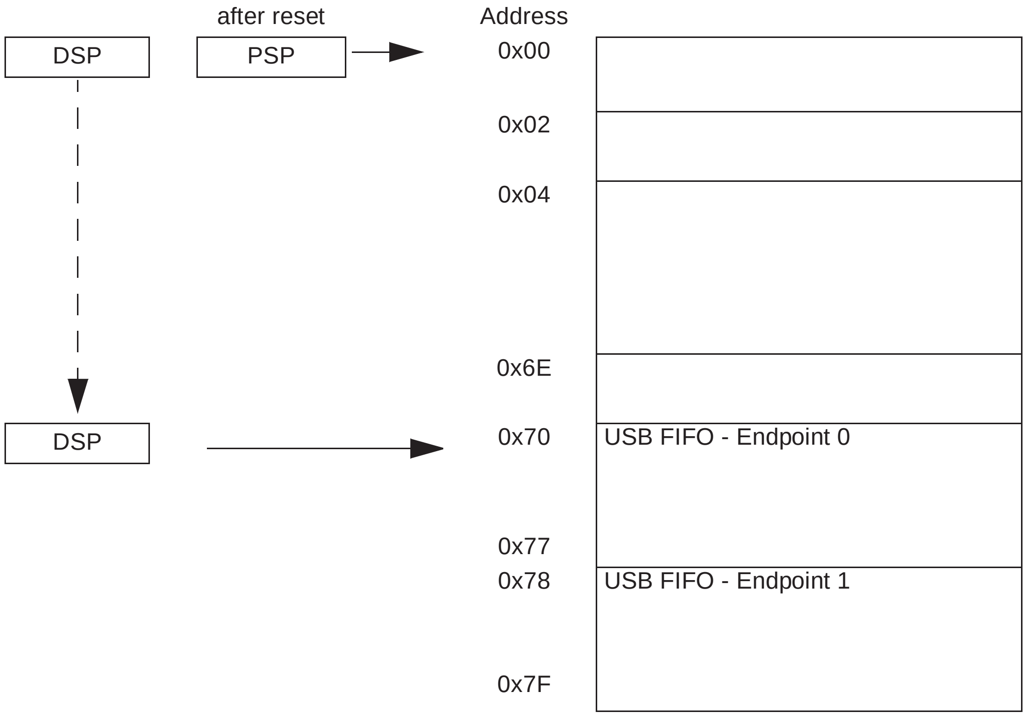


Figure 5-2. Data Memory Space

5.2 I/O Register Summary

I/O registers are accessed via the I/O Read (IORD) and I/O Write (IOWR, IOWX) instructions.

Table 5-1. I/O Register Summary

Register Name	I/O Address	Read/Write	Function
Port 0 Data	0x00	R/W	General purpose I/O Port (low current)
Port 1 Data	0x01	R/W	General purpose I/O Port (high current)
Port 0 Interrupt Enable	0x04	W	Interrupt enable for pins in Port 0
Port 1 Interrupt Enable	0x05	W	Interrupt enable for pins in Port 1
Port 0 Pull-up	0x08	W	Pull-up resistor control for Port 0 pins
Port 1 Pull-up	0x09	W	Pull-up resistor control for Port 1 pins
USB EP 0 TX Config.	0x10	R/W	USB End Point 0 transmit configuration
USB EP 1 TX Config.	0x11	R/W	USB End Point 1 transmit configuration
USB Device Address	0x12	R/W	USB device address
USB Status & Control	0x13	R/W	USB status and control
USB EP 0 RX Status	0x14	R/W	USB End Point 0 receive status

Table 5-1. I/O Register Summary (continued)

Register Name	I/O Address	Read/Write	Function
Global Interrupt Enable	0x20	R/W	Global Interrupt Enable
Watch Dog Timer	0x21	W	Watch Dog Timer clear
Cext Clear	0x22	R/W	External R-C Timing circuit control
Timer	0x23	R	Free-running timer
Port 0 Isink	0x30-0x37	W	Input sink current control for Port 0 pins. There is one Isink register for each pin. Address of the Isink register for pin 0 is located at 0x30 and the register address for pin 7 is located at 0x37
Port 1 Isink	0x38-0x3B	W	Input sink current control for Port 1 pins. There is one Isink register for each pin. Address of the Isink register for pin 0 is located at 0x38 and the register address for pin 3 is located at 0x3B
Status & Control	0xFF	R/W	Processor status and control

5.3 Reset

The USB Controller supports three types of resets. All registers are restored to their default states during a reset. The USB Device Address is set to 0 and all interrupts are disabled. In addition, the Program Stack Pointer (PSP) is set to 0x00 and the Data Stack Pointer (DSP) is set to 0x00. The user should set the DSP to location 0x70 to reserve 16 bytes of FIFO space. The assembly instructions to do so are:

```
Mov A, 70h     ; Move 70 hex into Accumulator, use 70 instead of 6F because the dsp is
               ; always decremented by 1 before data transfer in the PUSH instruction
Swap A, dsp    ; Move Accumulator value into dsp
```

The three reset types are:

1. Power On Reset (POR)
2. Watch Dog Reset (WDR)
3. USB Reset

The occurrence of a reset is recorded in the Status and Control Register located at I/O address 0xFF (*Figure 5-3*). Reading and writing this register are supported by the IORD and IOWR instructions. Bits 1, 2, and 7 are reserved and must be written as zeros during a write. During a read, reserved bit positions should be ignored. Bits 4, 5, and 6 are used to record the occurrence of POR, USB and WDR Reset respectively. The firmware can interrogate these bits to determine the cause of a reset. Bit 0 is the “Run” control, clearing this bit will stop the microcontroller. Once this bit is set to low, only a reset can set this bit HIGH.

The microcontroller resumes execution from ROM address 0X00 after a reset unless the Suspend bit (bit 3) of the Status and Control Register is set. Setting the Suspend bit stops the clock oscillator and the interrupt timers as well as powering-down the microcontroller. The detection of any USB activity will terminate the suspend condition.

7	6	5	4	3	2	1	0
W	R/W	R/W	R/W	R/W	W	W	R/W
Reserved	Watch Dog Reset	USB Reset	Power-on Reset	Suspend	Reserved	Reserved	Run

Figure 5-3. Status and Control Register (Address 0xFF)

5.3.1 Power-On Reset (POR)

Power On Reset (POR) occurs every time the power to the device is switched on. Bit 4 of the Status and Control Register is set to record this event (the register contents are set to 00011001 by the POR). The USB Controller is placed in suspended mode at the end of POR to conserve power (most device functions such as the clock oscillator, the timers, and the interrupt logic are turned off in the suspend mode). Only a non-idle USB Bus state will terminate the suspend mode and begin normal operations.

5.3.2 Watch Dog Reset (WDR)

The Watch Dog Timer Reset (WDR) occurs when the Most Significant Bit of the 4-bit Watch Dog Timer Register transitions from LOW to HIGH. Writing any value to the write-only Watch Dog Restart Register at 0x21 will clear the timer. The Watch Dog timer is clocked by a 1.024 ms clock from the free running timer. If 8 clocks occur between writes to the timer, a WDR occurs. Bit 6 of the Status and Control Register will be set to record the event. A Watch Dog Timer Reset lasts for 8.192 ms after which the microcontroller begins execution at ROM address 0x00. The USB transmitter is disabled by a Watch Dog Reset because the USB Device Address Register is cleared. Otherwise, the USB Controller would respond to all address 0 transactions. The transmitter remains disabled until the WDR bit in the Status and Control Register is reset to 0 by firmware.

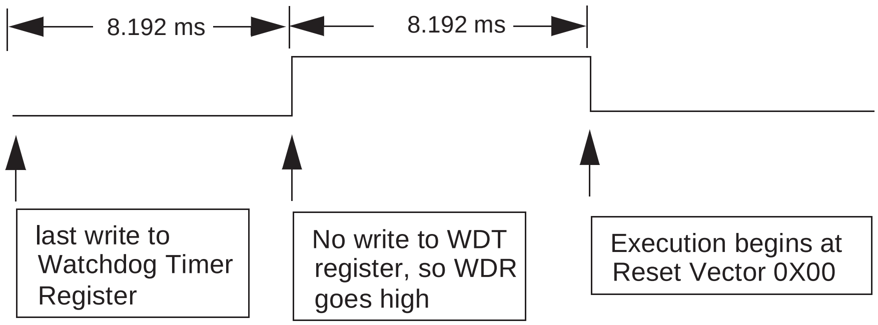


Figure 5-4. Watch Dog Reset (WDR)

5.3.3 USB Bus Reset

The USB Controller recognizes a USB Reset when a Single Ended Zero (SE0) condition persists for longer than 8 micro-seconds. SE0 is defined as the condition in which both the D+ line and the D– line are LOW. Bit 5 of the Status and Control Register will be set to record this event. If the USB reset happens while the device is suspended (such as after a POR), the suspend condition will be cleared and the clock oscillator will be restarted. However, the microcontroller is not released until the USB reset is removed.

5.4 On-chip Timer

The USB Controller is equipped with an 8-bit free-running timer driven by a clock one-sixth the crystal frequency. Bits 0 through 7 of the counter are readable from the read-only Timer Register located at I/O address 0x23. The Timer Register is cleared during a Power-On Reset. *Figure 5-5* illustrates the format of this register and *Figure 5-6* is its block diagram.

With a 6 MHz crystal, the timer resolution is 1 µs.

The timer generates two interrupts: the 128 µs interrupt and the 1.024 ms interrupt.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
Count 7	Count 6	Count 5	Count 4	Count 3	Count 2	Count 1	Count 0

Figure 5-5. Timer Register (Address 0x23)

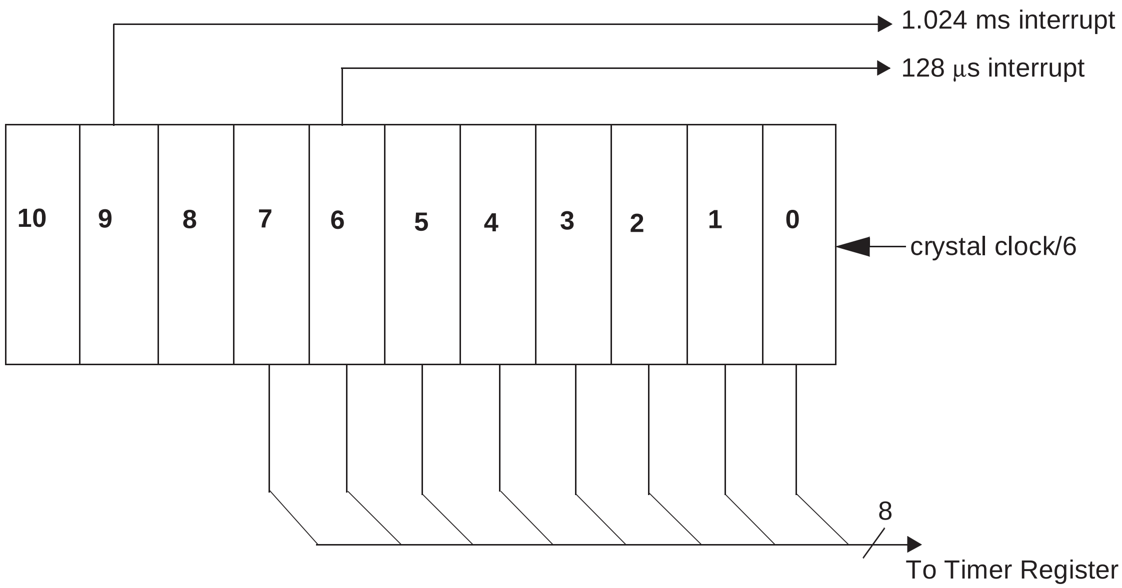


Figure 5-6. Timer Block Diagram

5.5 General Purpose I/O Ports

Interface with peripherals is conducted via 12 GPIO signals. These 12 signals are divided into two ports: Port 0 and Port 1. Port 0 contains eight lines (P0.0–P0.7) and Port 1 contains up to eigth lines (P1.0–P1.7), depending on the package. Both ports can be accessed by the IORD, IOWR and IOWX instructions. The Port 0 data register is located at I/O address 0x00 while the Port 1 data register is located at I/O address 0x01. The contents of both registers are set HIGH during a reset. Refer to *Figures 5-7* and *5-8* for the formats of the data registers. In addition to supporting general input/output functions, each I/O line can trigger an interrupt to the microcontroller. Please refer to the interrupt section for more details.

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Figure 5-7. Port 0 Data Register (Address 0x00)

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Figure 5-8. Port 1 Data Register (Address 0x01)

Each GPIO line includes an internal 16 KΩ resistor. This resistor provides both the pull-up function and slew control. Two factors govern the enabling and disabling of each resistor: the state of its associated Port Pull-up register bit and the state of the Data Register bit. The control bits in the Port Pull-up register are active LOW.

The output is HIGH when a “1” is written to the Data Register and the Port Pull-up register is “0”. Writing a “0” to the Data Register will disable the Pull-up resistor and output a LOW regardless of the setting in the Port Pull-up Register. The output will go to a high-Z state if the Data Register bit and the Port Pull-up Register bit are both “1”. *Figure 5-9* illustrates the block diagram of one I/O line. The Port Isink Register is used to control the output current level and it is described later in this section. *Table 5-2* is the Output Control truth table.

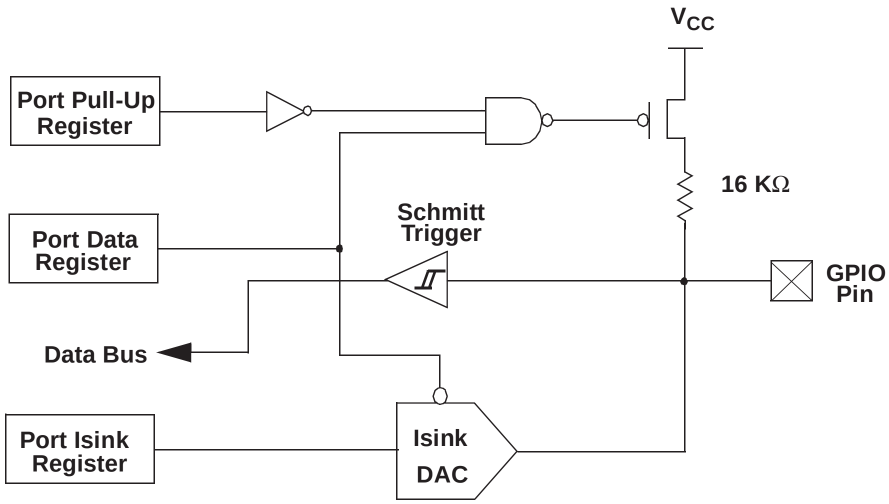


Figure 5-9. Block Diagram of an I/O Line

Table 5-2. Output Control Truth Table

Data Register	Port Pull-up Register	Output at I/O Pin
0	0	Sink Current (‘0’)
0	1	Sink Current (‘0’)
1	0	Pull-up Resistor (‘1’)
1	1	Hi-Z

To configure a GPIO pin as an input, a “1” should be written to the Port Data Register bit associated with that pin to disable the pull down function of the Isink DAC (see *Figure 5-9*).When the Port Data Register is read, the bit value will be a “1” if the voltage on the pin is greater than the Schmitt trigger threshold and “0” if below the threshold. In applications where an internal pull-up is required, the 16K-Ω pull-up resistor can be engaged by writing a “0” to the appropriate bit in the Port Pull-Up Register.

Both Port 0 and Port 1 Pull-up registers are write only (see *Figures 5-10* and *5-11*). Port 0 Pull-up is located at I/O address 0x08 and Port 1 Pull-up is mapped to address 0x09. The contents of the Port Pull-up registers are cleared during reset, allowing the outputs to be controlled by the state of the Data Registers. The Port pull-up registers also selects the polarity of transition that generates a GPIO interrupt. A “0” selects a HIGH to LOW transition while a “1” selects a LOW to HIGH transition.

7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W
Pull P0.7	Pull P0.6	Pull P0.5	Pull P0.4	Pull P0.3	Pull P0.2	Pull P0.1	Pull P0.0

Figure 5-10. Port 0 Pull-Up Register (Address 0x08)

7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W
Pull P1.7	Pull P1.6	Pull P1.5	Pull P1.4	Pull P1.3	Pull P1.2	Pull P1.1	Pull P1.0

Figure 5-11. Port 1 Pull-Up Register (Address 0x09)

Writing a “0” to the Data Register will drive the output LOW. Instead of providing a fixed output drive, the USB Controller allows the user to select an output sink current level for each I/O pin. The sink current of each output is controlled by a dedicated Port Isink Register. The lower 4 bits of this register contain a code selecting one of sixteen sink current levels. The upper 4 bits of the register are ignored. The format of the Port Isink Register is shown in *Figure 5-12*.

7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W
Isink7	Isink6	Isink5	Isink4	Isink3	Isink2	Isink1	Isink0

Figure 5-12. Port Isink Register for One GPIO Line

Port 0 is a low current port suitable for connecting photo transistors. Port 1 is a high current port capable of LED drive. See section 7.0 for current ranges. 0000 is the lowest drive strength. 1111 is the highest.

The write-only sink current control registers for Port 0 outputs are assigned from I/O address 0x30 to 0x37 with the control bits for P00 starting at 0x30. Port 1 sink current control registers continue from I/O address 0x38 to 0x3B. All sink current control registers are cleared during a reset, resulting in the minimum drive setting.

5.6 Instant-on Feature (Suspend Mode)

The USB Controller can be placed in a low-power state by setting the Suspend bit (bit 3) of the Status and Control register. Almost all logic blocks in the device are turned off except the USB receiver, the GPIO interrupt logic, and the Cext interrupt logic. The clock oscillator as well as the free-running and watch dog timers are shut down.

The suspend mode will be terminated when one of the three following conditions occur:

1. USB activity
2. A GPIO interrupt
3. Cext interrupt

The clock oscillator, GPIO and timers restart immediately on exiting suspend mode. The USB engine and microcontroller return to a fully functional state at most 256 us later. The microcontroller will execute the instruction following the I/O write that placed the device into suspend mode before servicing any interrupt requests.

Both the GPIO interrupt and the Cext interrupt allow the USB Controller to wake-up periodically and poll potentiometers, optics, and other system components while maintaining a very low average power consumption.

To use Cext to generate an “Instant-on” interrupt, the pin is connected to ground with an external capacitor and connected to VCC with an external resistor. A “0” is written to the Cext register located at I/O address 0x22 to discharge the capacitor. A “1” is then written to disable the open-drain output driver. A Schmitt trigger input circuit monitors the input and generates a wake-up interrupt when the input voltage rises above the input threshold. By changing the values of the external resistor and capacitor, the user can fine tune the charge rate of the R-C timing circuit. The format of the Cext register is shown in *Figure 5-13*. Reading the register returns the value of the Cext pin. During a reset, the Cext is HIGH.

7	6	5	4	3	2	1	0
							R/W
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Cext

Figure 5-13. The Cext Register (Address 0x22)

5.7 XTALIN/XTALOUT

XTALIN and XTALOUT are the crystal oscillator pins. A 6 MHz crystal or ceramic resonator should be connected to these pins.The feedback capacitors and bias resistor are internal to the IC.

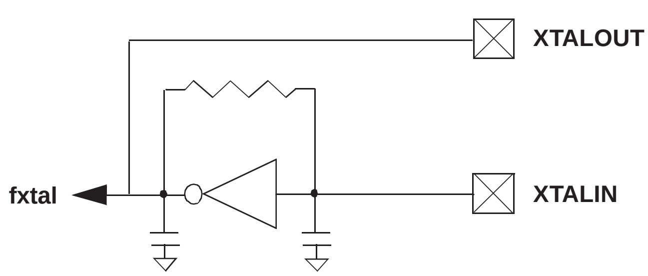


Figure 5-14. Clock Oscillator On-chip Circuit

5.8 Interrupts

Interrupts are generated by the General Purpose I/O lines, the Cext pin, the internal timer, and the USB engine. All interrupts except Reset are maskable by the Global Interrupt Enable Register. Access to this register is accomplished via IORD, IOWR and IOWX instructions to address 0x20. Writing a “1” to a bit position enables the interrupt associated with that position. During a reset, the contents the Interrupt Enable Register are cleared, disabling all interrupts. *Figure 5-15* illustrates the format of the Global Interrupt Enable Register.

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Wake-up Interrupt Enable	GPIO Interrupt Enable	Reserved	USB EP1 Interrupt Enable	USB EP0 Interrupt Enable	1.024 ms Interrupt Enable	128 us Interrupt Enable	Reserved

Figure 5-15. Global Interrupt Enable Register (Address 0x20)

The interrupt controller contains a separate latch for each interrupt except the Wake-up interrupt. When an interrupt is generated it is latched as a pending interrupt. It will stay as a pending interrupt until it is serviced or a reset occurs. The Wake-up interrupt is not latched, and is pending whenever the Cext pin is high. A pending interrupt will only generate an interrupt request if it is enabled in the Global Interrupt Enable Register. The highest priority interrupt request will be serviced following the execution of the current instruction.

When servicing an interrupt, the hardware will first disable all interrupts by clearing the Global Interrupt Enable Register. Next, the interrupt latch of the current interrupt is cleared. This is followed by a CALL instruction to the ROM address associated with the interrupt being serviced (i.e., the Interrupt Vector). The instruction in the interrupt table is typically a JMP instruction to the address of the Interrupt Service Routine (ISR). The user can re-enable interrupts in the interrupt service routine by writing to the appropriate bits in the Global Interrupt Enable Register. Interrupts can be nested to a level limited only by the available stack space.

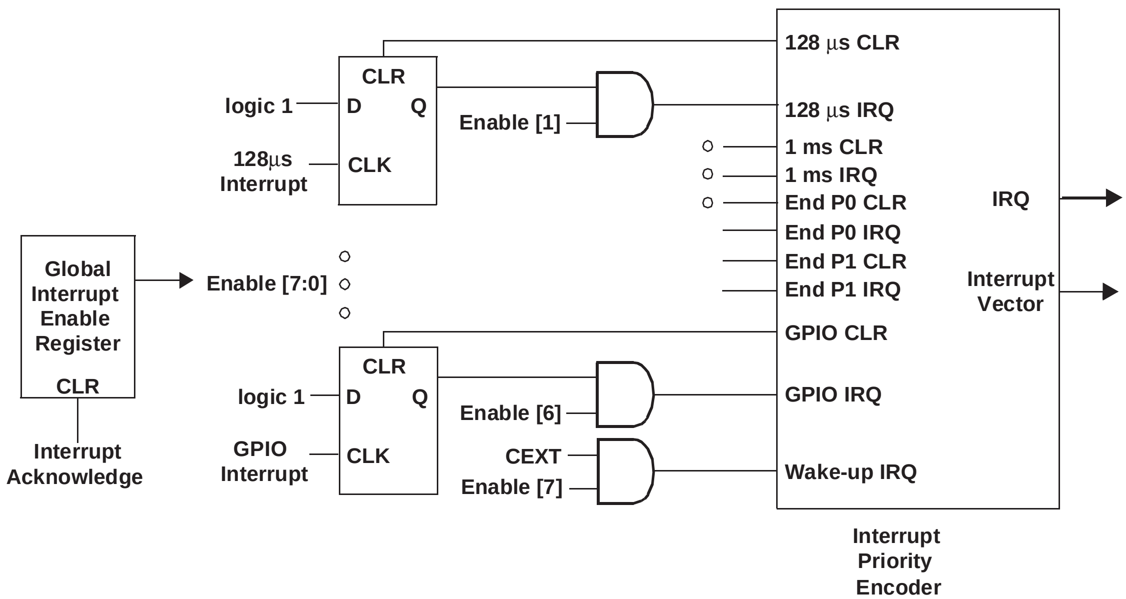


Figure 5-16. Interrupt Controller Logic Block Diagram

The Program Counter value as well as the Carry and Zero flags (CF, ZF) are automatically stored onto the Program Stack by the CALL instruction as part of the interrupt acknowledge process. The user firmware is responsible for insuring that the processor state is preserved and restored during an interrupt. For example the PUSH A instruction should be used as the first command in the ISR to save the accumulator value and the POP A instruction should be used just before the RET instruction to restore the accumulator value. The program counter CF and ZF are restored when the RET instruction is executed.

The Interrupt Vectors supported by the USB Controller are listed in *Table 5-3*. Interrupt Vector 0 (Reset) has the highest priority, Interrupt Vector 7 has the lowest priority. Because the JMP instruction is 2 bytes long, the interrupt vectors occupy 2 bytes.

Table 5-3. Interrupt Vector Assignments

Interrupt Vector Number	ROM Address	Function
0	0x00	Reset
1	0x02	128 µs timer interrupt
2	0x04	1.024 ms timer interrupt
3	0x06	USB end point 0 interrupt
4	0x08	USB end point 1 interrupt
5	0x0A	Reserved
6	0x0C	GPIO interrupt
7	0x0E	Wake-up interrupt

5.8.1 Interrupt Latency

Interrupt latency can be calculated from the following equation:

Interrupt Latency = (Number of clock cycles remaining in the current instruction) + (10 clock cycles for the CALL instruction) + (5 clock cycles for the JMP instruction)

For example, if a 5 clock cycle instruction such as JC is being executed when an interrupt occurs, the first instruction of the Interrupt Service Routine will execute a min. of 16 clocks (1+10+5) or a max. of 20 clocks (5+10+5) after the interrupt is issued. The interrupt latches are sampled at the rising edge of the last clock cycle in the current instruction.

5.8.2 GPIO Interrupt

The General Purpose I/O interrupts are generated by signal transitions at the Port 0 and Port 1 I/O pins. GPIO interrupts are edge sensitive with programmable interrupt polarities. Setting a bit HIGH in the Port Pull-up Register (see *Figure 5-10* and *5-11*) selects a LOW to HIGH interrupt trigger for the corresponding port pin. Setting a bit LOW activates a HIGH to LOW interrupt trigger. Each GPIO interrupt is maskable on a per-pin basis by a dedicated bit in the Port Interrupt Enable Register. Writing a “1” enables the interrupt. *Figure 5-17* and *Figure 5-18* illustrate the format of the Port Interrupt Enable Registers for Port 0 and Port 1 located at I/O address 0x04 and 0x05 respectively. These write only registers are cleared during reset, thus disabling all GPIO interrupts.

7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W
P0.7 Int En	P0.6 Int En	P0.5 Int En	P0.4 Int En	P0.3 Int En	P0.2 Int En	P0.1 Int En	P0.0 Int En

Figure 5-17. Port 0 Interrupt Enable Register (Address 0x04)

7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W
P1.7 Int En	P1.6 Int En	P1.5 Int En	P1.4 Int En	P1.3 Int En	P1.2 Int En	P1.1 Int En	P1.0 Int En

Figure 5-18. Port 1 Interrupt Enable Register (Address 0x05)

A block diagram of the GPIO interrupt logic is shown in *Figure 5-19*. The bit setting in the Port Pull-up Register selects the interrupt polarity. If the selected signal polarity is detected on the I/O pin a HIGH signal is generated. If the Port Interrupt Enable bit for this pin is HIGH and no other port pins are requesting interrupts, then the 12-input OR gate will issue a LOW to HIGH signal to clock the GPIO interrupt flip flop. The output of the flip flop is further qualified by the Global GPIO Interrupt Enable bit before it is processed by the Interrupt Priority Encoder. Both the GPIO interrupt flip flop and the Global GPIO Enable bit are cleared during GPIO interrupt acknowledge by on-chip hardware.

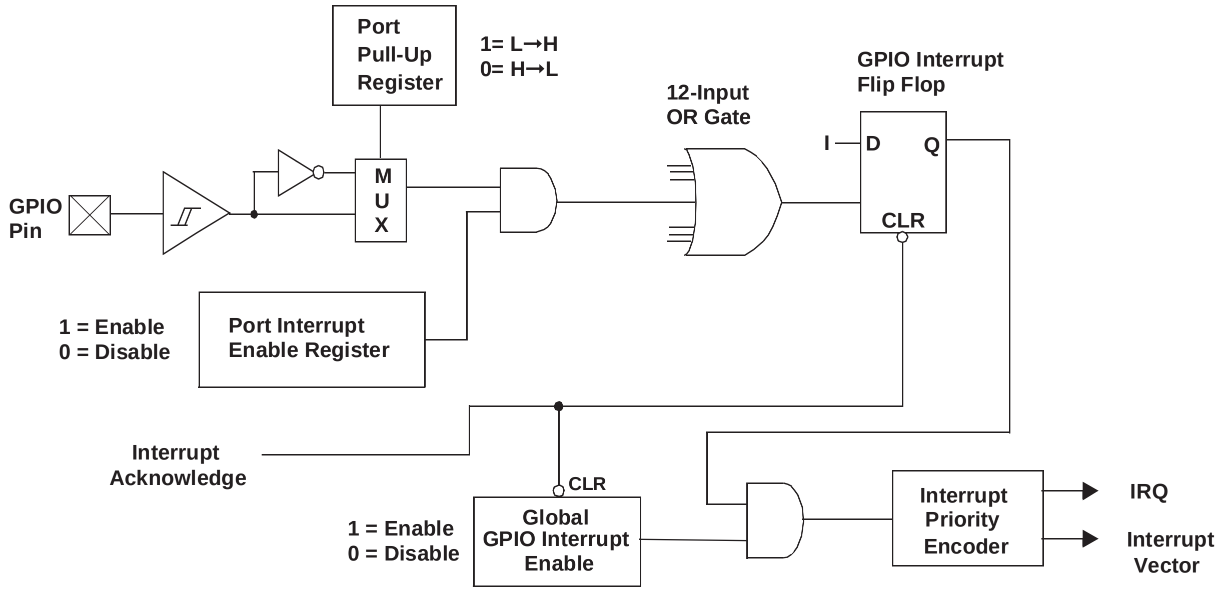


Figure 5-19. GPIO Interrupt Logic Block Diagram

Please note that if one port pin triggered an interrupt, no other port pins can cause a GPIO interrupt until that port pin has returned to its inactive (non-trigger) state or its corresponding port interrupt enable bit is cleared. The USB Controller does not assign interrupt priority to different port pins and the Port Interrupt Enable Registers are not cleared during the interrupt acknowledge process. When a GPIO interrupt is serviced, the ISR must poll the ports to determine which pin caused the interrupt.

5.8.3 USB Interrupt

A USB End Point 0 interrupt is generated after the host has written data to End Point 0 or after the USB Controller has transmitted a packet from End Point 0 and receives an ACK from the host. An OUT packet from the host which is NAKd by the USB Controller will not generate an interrupt. This interrupt is masked by the USB EP0 Interrupt Enable bit (bit 3) of the Global Interrupt Enable Register.

A USB End Point 1 interrupt is generated after the USB Controller has transmitted a packet from End Point 1 and has received an ACK from the host. This interrupt is masked by the USB EP1 Interrupt Enable bit (bit 4) of the Global Interrupt Enable Register.

5.8.4 Timer Interrupt

There are two timer interrupts: the 128 µs interrupt and the 1.024 ms interrupt. They are masked by bits 1 and 2 of the Global Interrupt Enable Register respectively. The user should disable both timer interrupts before going into the suspend mode to avoid possible conflicts between servicing the interrupts first or the suspend request first.

5.8.5 Wake-up Interrupt

A wake-up interrupt is generated when the Cext pin is HIGH. It is level sensitive and is not latched to the interrupt controller. It can be masked by the Wake-up Interrupt Enable bit (bit 7) of the Global Interrupt Enable Register. This interrupt can be used to perform periodic checks on attached peripherals when the USB Controller is placed in the low-power suspend mode. See the Instant-On Feature section for more details.

5.9 USB Engine

The USB engine includes the Serial Interface Engine (SIE) and the low-speed USB I/O transceivers. The SIE block performs most of the USB interface functions with only minimal support from the microcontroller core. Two end points are supported. End Point 0 is used to receive and transmit control (including setup) packets while End Point 1 is only used to transmit data packets.

The USB SIE processes USB bus activity at the transaction level independently. It does all the NRZI encoding/decoding and bit stuffing/unstuffing. It also determines token type, checks address and endpoint values, generates and checks CRC values and controls the flow of data bytes between the bus and the End Point FIFOs.

The firmware handles higher level and function specific tasks. During control transfers the firmware must interpret device requests and respond correctly. It also must coordinate Suspend/Resume, verify and select DATA toggle values, and perform function specific tasks.

The USB engine and the firmware communicate though the End Point FIFOs, USB End Point interrupts, and the USB registers described in the sections below.

5.9.1 USB Enumeration Process

The USB Controller provides a USB Device Address Register at I/O location 0x12. Reading and writing this register is achieved via the IORD and IOWR instructions. The register contents are cleared during a reset, setting the USB address of the USB Controller to 0. *Figure 5-20* shows the format of the USB Address Register.

7	6	5	4	3	2	1	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reserved	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0

Figure 5-20. USB Device Address Register (Address 0x12)

Typical enumeration steps:

1. The host computer sends a SETUP packet followed by a DATA packet to USB address 0 requesting the Device descriptor.
2. The USB Controller decodes the request and retrieves its Device descriptor from the program memory space.
3. The host computer performs a control read sequence and the USB Controller responds by sending the Device descriptor over the USB bus.
4. After receiving the descriptor, the host computer sends a SETUP packet followed by a DATA packet to address 0 assigning a new USB address to the device.
5. The USB Controller stores the new address in its USB Device Address Register after the no-data control sequence completes.
6. The host sends a request for the Device descriptor using the new USB address.
7. The USB Controller decodes the request and retrieves the Device descriptor from the program memory.
8. The host performs a control read sequence and the USB Controller responds by sending its Device descriptor over the USB bus.
9. The host generates control reads to the USB Controller to request the Configuration and Report descriptors.
10. The USB Controller retrieves the descriptors from its program space and returns the data to the host over the USB.
11. Enumeration is complete after the host has received all the descriptors.

5.9.2 End Point 0

All USB devices are required to have an end point number 0 that is used to initialize and manipulate the device. End Point 0 provides access to the device's configuration information and allows generic USB status and control accesses.

End Point 0 can receive and transmit data. Both receive and transmit data share the same 8-byte End Point 0 FIFO located at data memory space 0x70 to 0x77. Received data may overwrite the data previously in the FIFO.

5.9.2.1 End Point 0 Receive

After receiving a packet and placing the data into the End Point 0 FIFO, the USB Controller updates the USB End Point 0 RX register to record the receive status and then generates an USB End Point 0 interrupt. The format of the End Point 0 RX Register is shown in *Figure 5-21*.

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Count 3	Count 2	Count 1	Count 0	Data Toggle	IN	OUT	SETUP

Figure 5-21. USB End Point 0 RX Register (Address 0x14)

This is a read/write register located at I/O address 0x14. Any write to this register will clear all bits except bit 3 which remains unchanged. All bits are cleared during reset.

Bit 0 is set to 1 when a SETUP token for End Point 0 is received. Once set to a 1 this bit remains high until it is cleared by an I/O write or a reset. While the data following a SETUP is being received by the USB engine, this bit will not be cleared by an I/O write. User firmware writes to the USB FIFOs are disabled when bit 0 is set. This prevents SETUP data from being overwritten.

Bits 1 and 2 are updated whenever a valid token is received on End Point 0. Bit 1 is set to 1 if an OUT token is received and cleared to 0 if any other token is received. Bit 2 is set to 1 if an IN token is received and cleared to 0 if any other token i s received.

Bit 3 shows the Data Toggle status of DATA packets received on End Point 0. This bit is updated for DATA following SETUP tokens and for DATA following OUT tokens if Stall (bit 5 of 0x10) is not set and either EnableOuts or StatusOuts (bits 3 and 4 of 0x13) are set.

Bits 4 to 7 are the count of the number of bytes received in a DATA packet. The two CRC bytes are included in the count, so the count value is two greater than the number of data bytes received. The count is always updated and the data is always stored in the FIFO for DATA packets following a SETUP token. The count for DATA following an OUT token is updated if Stall (bit 5 of 0x10) is 0 and either EnableOuts or StatusOuts (bits 3 and 4 of 0x13) are 1. The DATA following an OUT will be written into the FIFO if EnableOuts is set to 1 and Stall and StatusOuts are 0.

A maximum of 8 bytes are written into the End Point 0 FIFO. If there are less the 8 bytes of data the CRC is written into the F IFO.

Due to register space limitations, the Receive Data Invalid bit is located in the USB End Point 0 TX Configuration Register. Refer to the End Point 0 Transmit section for details. This bit is set by the SIE if an error is detected in a received DATA packet.

The table below summarizes the USB Engine response to SETUP and OUT transactions on End Point 0. In the Data Packet column ‘Error’ represents a packet with a CRC, PID or bit stuffing error, or a packet with more than 8 bytes of data. ‘Valid’ is a packet without an Error. ‘Status’ is a packet that is a valid control read Status stage, while ‘N/Status’ is not a correct Status stage (see section 5.9.4). The ‘Stall’ bit is described is section 5.9.2.2. The ‘StatusOuts’ and ‘EnableOuts’ bits are described in section 5.9.4.

Control Bit Settings			Received Packets		USB Engine Response				
Stall	Status Out	Enable Out	Token Type	Data Packet	FIFO Write	Toggle Update	Count Update	Interrupt	Reply
-	-	-	SETUP	Valid	Yes	Yes	Yes	Yes	ACK
-	-	-	SETUP	Error	Yes	Yes	Yes	Yes	None
0	0	1	OUT	Valid	Yes	Yes	Yes	Yes	ACK
0	0	1	OUT	Error	Yes	Yes	Yes	Yes	None
0	0	0	OUT	Valid	No	No	No	No	NAK
0	0	0	OUT	Error	No	No	No	No	None
1	0	0	OUT	Valid	No	No	No	No	STALL
1	0	0	OUT	Error	No	No	No	No	None
0	1	0	OUT	Status	No	Yes	Yes	Yes	ACK
0	1	0	OUT	N/Status	No	Yes	Yes	Yes	STALL
0	1	0	OUT	Error	No	Yes	No	No	None

Figure 5-22. USB Engine Response to SETUP and OUT transactions on End Point 0

5.9.2.2 End Point 0 Transmit

The USB End Point 0 TX Register located at I/O address 0x10 controls data transmission from End Point 0 (see *Figure 5-23*). This is a read/write register. All bits are cleared during reset.

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Enable Respond to IN packets	Data 1/0	Stall	Data Invalid	Count 3	Count 2	Count 1	Count 0

Figure 5-23. USB End Point 0 TX Configuration Register (Address 0x10)

Bits 0 to 3 indicate the numbers of data bytes to be transmitted during an IN packet, valid values are 0 to 8 inclusive.

Bit 4 indicates that a received DATA packet error (CRC, PID, or bitstuffing error) occurred during a SETUP or OUT data phase.

Setting the Stall bit (bit 5) will stall IN and OUT packets. This bit is cleared whenever a SETUP packet is received by End Point 0.

Bit 6 (Data 1/0) must be set to either 0 or 1 to select the DATA packet’s toggle state, 0 for DATA0, 1 for DATA1.

After the transmit data has been loaded into the FIFO, bit 6 should be set according to the data toggle state and bit 7 set to “1”. This enables the USB Controller to respond to an IN packet. Bit 7 is cleared and an End Point 0 interrupt is generated by the SIE once the host acknowledges the data transmission. Bit 7 is also cleared when a SETUP token is received. The Interrupt Service Routine can check bit 7 to confirm that the data transfer was successful.

5.9.3 End Point 1

End Point 1 is capable of transmit only. The data to be transmitted is stored in the 8-byte End Point 1 FIFO located at data memory space 0x78 to 0x7F.

5.9.3.1 End Point 1 Transmit

Transmission is controlled by the USB End Point 1 TX Register located at I/O address 0x11 (see *Figure 5-24*). This is a read/write register. All bits are cleared during reset.

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Enable Respond to IN packets	Data 1/0	Stall	End Point 1 Enable	Count 3	Count 2	Count 1	Count 0

Figure 5-24. USB End Point 1 TX Configuration Register (Address 0x11)

Bits 0 to 3 indicate the numbers of data bytes to be transmitted during an IN packet, valid values are 0 to 8 inclusive.

Bit 4 must be set before End Point 1 can be used. If this bit is cleared, the USB Controller will ignore all traffic to End Point 1.

Setting the Stall bit (bit 5) will stall IN and OUT packets until this bit is cleared.

Bit 6 (Data 1/0) must be set to either 0 or 1 depending on the data packet’s toggle state, 0 for DATA0, 1 for DATA1.

After the transmit data has been loaded into the FIFO, bit 6 should be set according to the data toggle state and bit 7 set to “1”. This enables the USB Controller to respond to an IN packet. Bit 7 is cleared and an End Point 1 interrupt is generated by the SIE once the host acknowledges the data transmission.

5.9.4 USB Status and Control

USB status and control is regulated by USB Status and Control Register located at I/O address 0x13 as shown in *Figure 5-25*. This is a read/write register. All reserved bits must be written to zero. All bits in the register are cleared during reset.

7	6	5	4	3	2	1	0
			R/W	R/W		R/W	R/W
Reserved	Reserved	Reserved	Enable Outs	StatusOuts	Reserved	Force Resume	Bus Activity

Figure 5-25. USB Status and Control Register (Address 0x13)

Bit 0 will be set by the SIE if any USB activity except idle (D+ LOW, D– HIGH) is detected. The user program should check and clear this bit periodically to detect any loss of bus activity. Writing a 0 to this bit clears it. Writing a 1 does not change its value.

Bit 1 is used to force the on-chip USB transmitter to the K state which will send a Resume signal to the host.

Bit 2 is a reserved bit that must be set to 0.

Bit 3 is used to automatically respond to the Status stage OUT of a control read transfer on End Point 0. A valid Status stage OUT contains a DATA1 packet with 0 bytes of data. If the StatusOuts bit is set, the USB engine will respond to a valid Status stage OUT with an ACK, and any other OUT with a STALL. The data is not written into the FIFO when this bit is set. This bit is cleared when a SETUP token is received by End Point 0.

Bit 4 is used to enable the receiving of End Point 0 OUT packets. When this bit is set to 1, the data from an OUT transaction to be written into the End Point 0 FIFO and the USB engine responds with an ACK. If this bit is 0, data will not be written to the FIFO and the response is a NAK. This bit is cleared following a SETUP or OUT transaction.

5.10 Instruction Set Summary

Table 5-4. Instruction Set Map

MNEMONIC	operand	opcode	cycles		MNEMONIC	operand	opcode	cycles
HALT		00	7		NOP		20	4
ADD A,expr	data	01	4		INC A	acc	21	4
ADD A,[expr]	direct	02	6		INC X	x	22	4
ADD A,[X+expr]	index	03	7		INC [expr]	direct	23	7
ADC A,expr	data	04	4		INC [X+expr]	index	24	8
ADC A,[expr]	direct	05	6		DEC A	acc	25	4
ADC A,[X+expr]	index	06	7		DEC X	x	26	4
SUB A,expr	data	07	4		DEC [expr]	direct	27	7
SUB A,[expr]	direct	08	6		DEC [X+expr]	index	28	8
SUB A,[X+expr]	index	09	7		IORD expr	address	29	5
SBB A,expr	data	0A	4		IOWR expr	address	2A	5
SBB A,[expr]	direct	0B	6		POP A		2B	4
SBB A,[X+expr]	index	0C	7		POP X		2C	4
OR A,expr	data	0D	4		PUSH A		2D	5
OR A,[expr]	direct	OE	6		PUSH X		2E	5
OR A,[X+expr]	index	0F	7		SWAP A,X		2F	5
AND A,expr	data	10	4		SWAP A,DSP		30	5
AND A,[expr]	direct	11	6		MOV [expr],A	direct	31	5
AND A,[X+expr]	index	12	7		MOV [X+expr],A	index	32	6
XOR A,expr	data	13	4		OR [expr],A	direct	33	7
XOR A,[expr]	direct	14	6		OR [X+expr],A	index	34	8
XOR A,[X+expr]	index	15	7		AND [expr],A	direct	35	7
CMP A,expr	data	16	5		AND [X+expr],A	index	36	8
CMP A,[expr]	direct	17	7		XOR [expr],A	direct	37	7
CMP A,[X+expr]	index	18	8		XOR [X+expr],A	index	38	8
MOV A,expr	data	19	4		IOWX [X+expr]	index	39	6
MOV A,[expr]	direct	1A	5		CPL		3A	4
MOV A,[X+expr]	index	1B	6		ASL		3B	4
MOV X,expr	data	1C	4		ASR		3C	4
MOV X,[expr]	direct	1D	5		RLC		3D	4
IPRET	addr	1E	13		RRC		3E	4
XPAGE		1F	4		RET		3F	8
JMP	addr	8x	5		JC	addr	Cx	5
CALL	addr	9x	10		JNC	addr	Dx	5
JZ	addr	Ax	5		JACC	addr	Ex	7
JNZ	addr	Bx	5		INDEX	addr	Fx	14

6.0 Absolute Maximum Ratings

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–0°C to +70°C
Supply voltage on V_{CC} relative to V_{SS}	–0.5V to +7.0V
DC input voltage	–0.5V to $+V_{CC}$+0.5V
DC voltage applied to outputs in High Z state	–0.5V to $+V_{CC}$+0.5V
Max. output current into Port 1 pins	60 mA
Max. output current into non-Port 1 pins	10 mA
Power dissipation	300 mW
Static discharge voltage	>2000V
Latch-up current	>200 mA

7.0 DC Characteristics Fosc = 6 MHz; Operating Temperature = 0 to 70°C

	Parameter	Min	Max	Units	Conditions
	General				
V_{cc}	Operating Voltage	4.0	5.25	V	
V_{max}	Maximum applied voltage	–0.5	6.5	V	
I_{CC}	V_{cc} Operating Supply Current		50	mA	
I_{SB1}	Supply Current - Suspend Mode		100	µA	Oscillator off, D– > Voh min
I_{SB2}	Supply Current - Start-up Mode		4	mA	V_{cc} = 5.0V
V_{pp}	Programming Voltage (disabled)	–0.4	0.4	V	
t_{start}	Resonator Start-up Interval		256	µs	V_{cc} = 5.0V, ceramic resonator
t_{int1}	Internal timer #1 interrupt period	128	128	µs	
t_{int2}	Internal timer #2 interrupt period	1.024	1.024	ms	
t_{watch}	WatchDog timer period	7.168	8.192	ms	
	Power On Reset				
V_{rst}	POR Voltage	2.0	3.4	V	NOTE [2, 6]
t_{vccs}	VCC reset slew	0.5	100	ms	linear ramp V_{CC}: 0 to Vrst
	USB Interface				
V_{oh}	Static Output High	2.8	3.6	V	15k ± 5% Ω to Gnd [3, 4]
V_{ol}	Static Output Low		0.3	V	NOTE 4
	General Purpose I/O				
R_{up}	Pull-up resistance	8K	24K	Ωs	
$I_{sink0(0)}$	Port 0 sink current (0), lowest current	0.1	0.3	mA	Vout = 2.0 V DC, Port 0 only [4]
$I_{sink0(F)}$	Port 0 sink current (F), highest current	0.5	1.5	mA	Vout = 2.0 V DC, Port 0 only [4]
$I_{sink1(0)}$	Port 1 sink current (0), lowest current	1.6	4.8	mA	Vout = 2.0 V DC, Port 1 only [4]
$I_{sink1(F)}$	Port 1 sink current (F), highest current	8	24	mA	Vout = 2.0 V DC, Port 1 only [4]
I_{range}	Sink current max/min	4.5	5.5		Vout = 2.0 V DC, Port 0 or 1 [1, 10]
I_{lin}	Differential nonlinearity		0.5	lsb	Port 0 or Port 1 [5]
I_{il}	Input leakage current		50	nA	CEXT only
I_{ol}	Sink current	6	18	mA	CEXT only

Notes:
1. Per Table 7-6 of revision 1.0 of USB specification, for Cload of 100–350pF.
2. Power on Reset will occur until the voltage on V_{CC} increases above Vrst.
3. Rx: external idle resistor, 7.5 KΩ, 2%, to V_{CC}.

7.0 DC Characteristics (continued) Fosc = 6 MHz; Operating Temperature = 0 to 70°C

	Parameter	Min	Max	Units	Conditions
t_{sink}	Current sink response time		0.8	µs	Full scale transition
	General Purpose I/O (continued)				
T_{ratio}	Tracking Ratio Port1 to Port0	13.6	18.4		Vout = 2.0V[9]
I_{max}	Port 1 max sink current		60	mA	Summed over all Port 1 bits
P_{max}	Port 1 & CEXT sink mode dissipation		25	mW	Per pin
V_{ith}	Input Threshold Voltage	45%	65%	Vcc	All ports and Cext [7]
V_H	Input Hysteresis Voltage	6%	12%	Vcc	All ports and Cext [8]
V_{OL1}	Output LOW Voltage, Cext pin		0.4	V	V_{CC} = Min., I_{OL} = 2mA
V_{OL2}	Output LOW Voltage, Cext pin		2.0	V	V_{CC} = Min., I_{OL} = 5mA

8.0 Switching Characteristics

Parameter	Description	Min.	Max.	Unit
t_{CYC}	Input clock cycle time	166.67	166.67	ns
t_{CH}	Clock HIGH time	0.45 t_{CYC}		ns
t_{CL}	Clock LOW time	0.45 t_{CYC}		ns
t_r	Transition Rise Time [1, 4, 8]	75	300	ns
t_f	Transition Fall Time [1, 4, 8]	75	300	ns

Notes:

4. 4.35 V to 5.25 V V_{CC}.
5. Measured as largest step size vs nominal according to measured full scale and zero programmed values.
6. POR can occur only once per applied V_{CC}, if V_{CC} drops below Vrst, POR will **not** re-occur. V_{CC} must return to 0.0V before POR will be re-applied on a subsequent V_{CC} ramp.
7. Low to High transition
8. This parameter is guaranteed, but not tested.
9. $T_{ratio} = I_{sink1(n)}/I_{sink0(n)}$ for the same n
10. $I_{range} = I_{sink(F)}/I_{sink(O)}$ for port 0 or 1 output

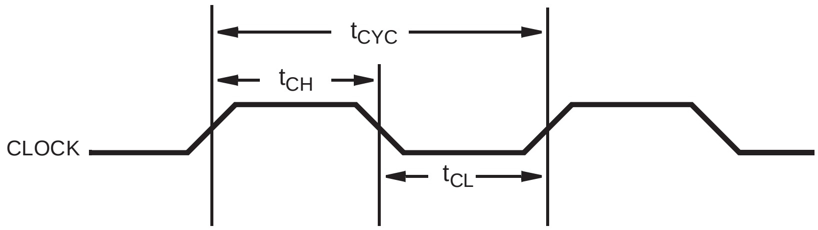


Figure 8-1. Clock Timing

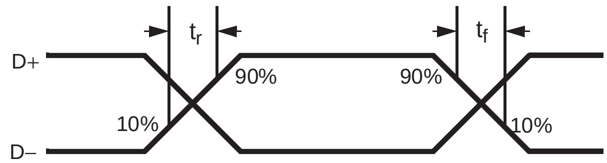


Figure 8-2. USB Data Signal Timing

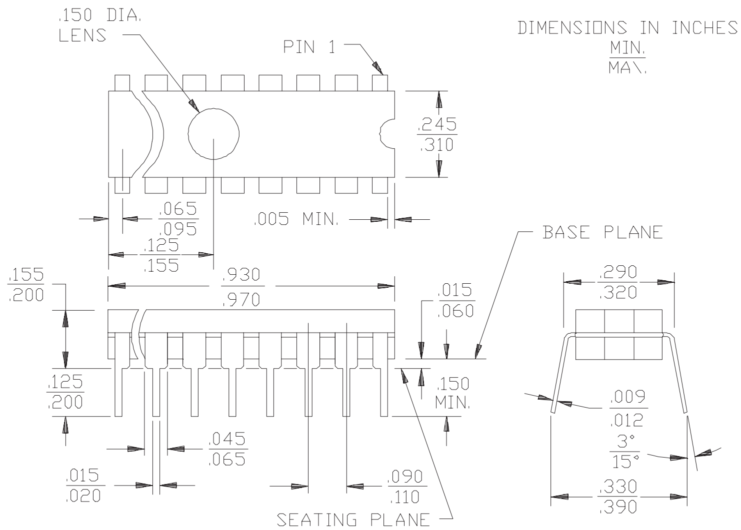
9.0 Ordering Information

Ordering Code	EPROM Size	Number of GPIO	Package Type	Operating Range
CY7C63000-PC	2KB	12	20-Pin (300-Mil) PDIP	Commercial
CY7C63000-SC	2KB	12	20-Pin (300-Mil) SOIC	Commercial
CY7C63001-PC	4KB	12	20-Pin (300-Mil) PDIP	Commercial
CY7C63001-SC	4KB	12	20-Pin (300-Mil) SOIC	Commercial
CY7C63001-WC	4KB	12	20-Pin (300-Mil) Windowed CerDIP	Commercial
CY7C63100-SC	2KB	16	24-Pin (300-Mil) SOIC	Commercial
CY7C63101-SC	4KB	16	24-Pin (300-Mil) SOIC	Commercial
CY7C63101-WC	4KB	16	24-Pin (300-Mil) Windowed CerDIP	Commercial
CY7C63200-PC	2KB	10	18-Pin (300-Mil) PDIP	Commercial
CY7C63201-PC	4KB	10	18-Pin (300-Mil) PDIP	Commercial
CY7C63201-WC	4KB	10	18-Pin (300-Mil) Windowed CerDIP	Commercial

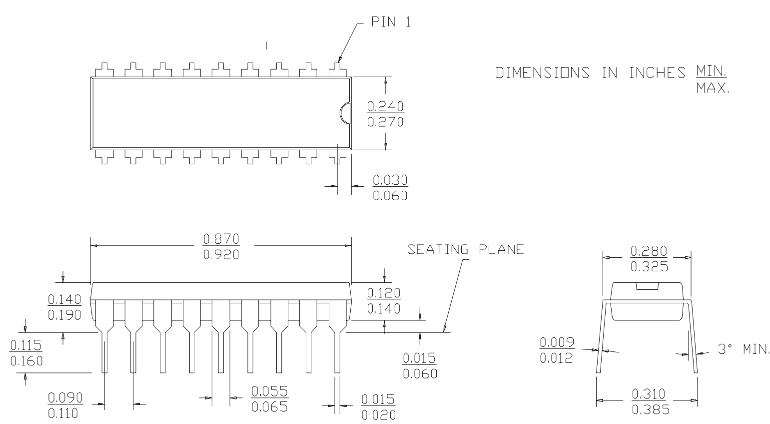
Document #: 38-00557-D

Package Diagrams

20-Lead (300-Mil) Windowed CerDIP W6
MIL-STD-1835 D-8 Config. A

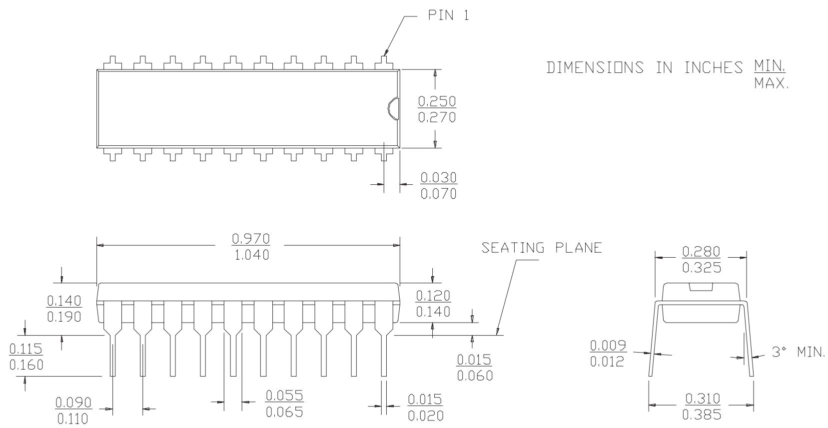


18-Lead (300-Mil) Molded DIP

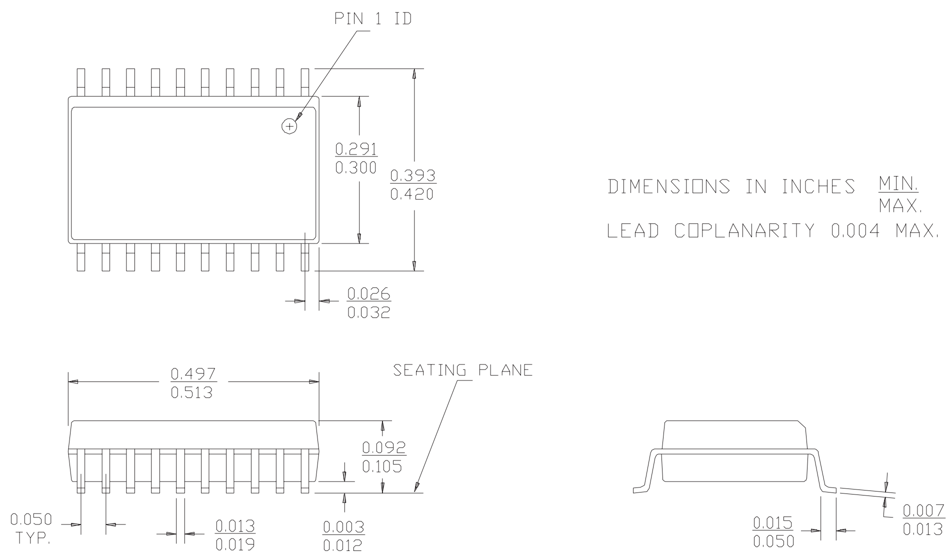


Package Diagrams (continued)

20-Lead (300-Mil) Molded DIP

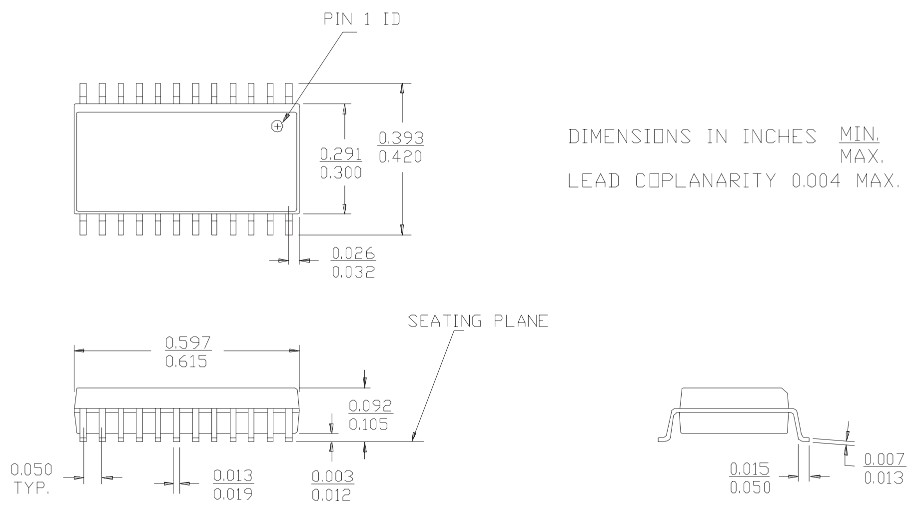


20-Lead (300-Mil) Molded SOIC

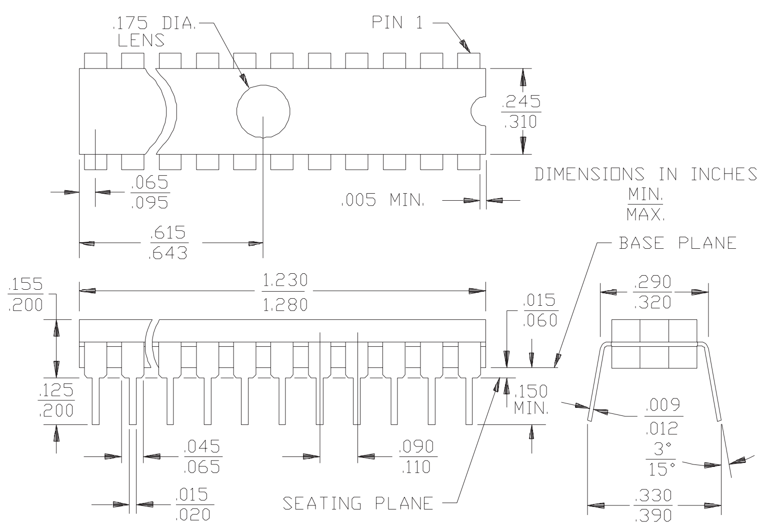


Package Diagrams (continued)

24-Lead (300-Mil) Molded SOIC



24-Lead (300-Mil) Windowed CerDIP W14
MIL-STD-1835 D-9 Config. A



Single Supply, Rail to Rail Low Power FET-Input Op Amp

AD820

FEATURES
True Single Supply Operation
- **Output Swings Rail-to-Rail**
- **Input Voltage Range Extends Below Ground**
- **Single Supply Capability from 5 V to 36 V**
- **Dual Supply Capability from ±2.5 V to ±18 V**

Excellent Load Drive
- **Capacitive Load Drive Up to 350 pF**
- **Minimum Output Current of 15 mA**

Excellent AC Performance for Low Power
- **800 μA Max Quiescent Current**
- **Unity Gain Bandwidth: 1.8 MHz**
- **Slew Rate of 3.0 V/μs**

Excellent DC Performance
- **800 μV Max Input Offset Voltage**
- **1 μV/°C Typ Offset Voltage Drift**
- **25 pA Max Input Bias Current**

Low Noise
- **13 nV/√Hz @ 10 kHz**

APPLICATIONS
Battery-Powered Precision Instrumentation
Photodiode Preamps
Active Filters
12- to 14-Bit Data Acquisition Systems
Medical Instrumentation
Low Power References and Regulators

PRODUCT DESCRIPTION

The AD820 is a precision, low power FET input op amp that can operate from a single supply of 5.0 V to 36 V, or dual supplies of ±2.5 V to ±18 V. It has true single supply capability with an input voltage range extending below the negative rail, allowing the AD820 to accommodate input signals below ground in the single supply mode. Output voltage swing extends to within 10 mV of each rail providing the maximum output dynamic range.

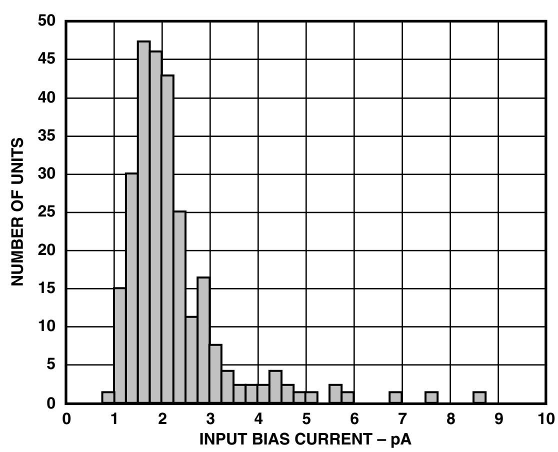
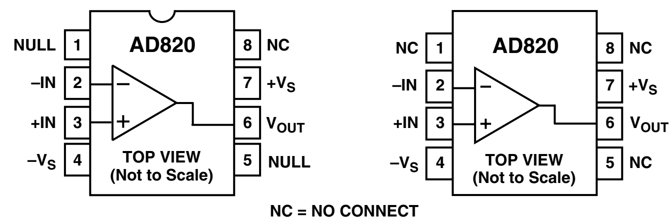


Figure 1. Typical Distribution of Input Bias Current

FUNCTIONAL BLOCK DIAGRAM



Offset voltage of 800 μV max, offset voltage drift of 1 μV/°C, typical input bias currents below 25 pA and low input voltage noise provide dc precision with source impedances up to a Gigaohm. 1.8 MHz unity gain bandwidth, –93 dB THD at 10 kHz and 3 V/μs slew rate are provided for a low supply current of 800 μA. The AD820 drives up to 350 pF of direct capacitive load and provides a minimum output current of 15 mA. This allows the amplifier to handle a wide range of load conditions. This combination of ac and dc performance, plus the outstanding load drive capability, results in an exceptionally versatile amplifier for the single supply user.

The AD820 is available in two performance grades. The A and B grades are rated over the industrial temperature range of –40°C to +85°C.

The AD820 is offered in two varieties of 8-lead package: plastic DIP, and surface mount (SOIC).

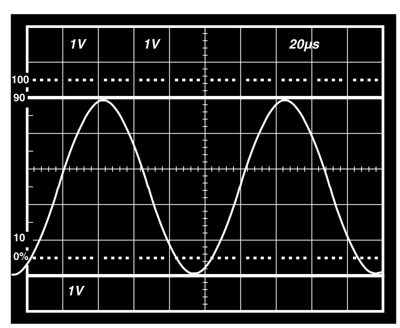


Figure 2. Gain of 2 Amplifier; V_S = 5, 0, V_{IN} = 2.5V Sine Centered at 1.25 Volts

REV. D

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

AD820—SPECIFICATIONS (V_S = 0, 5 V @ T_A = 25°C, V_{CM} = 0 V, V_{OUT} = 0.2 V unless otherwise noted.)

Parameter	Conditions	AD820A Min	AD820A Typ	AD820A Max	AD820B Min	AD820B Typ	AD820B Max	Unit
DC PERFORMANCE								
Initial Offset			0.1	0.8		0.1	0.4	mV
Max Offset over Temperature			0.5	1.2		0.5	0.9	mV
Offset Drift			2			2		μV/°C
Input Bias Current	V_O = 0 V to 4 V		2	25		2	10	pA
at T_{MAX}			0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
at T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_O = 0.2 V to 4 V							
T_{MIN} to T_{MAX}	R_L = 100 kΩ	400	1000		500	1000		V/mV
		400			400			V/mV
T_{MIN} to T_{MAX}	R_L = 10 kΩ	80	150		80	150		V/mV
		80			80			V/mV
T_{MIN} to T_{MAX}	R_L = 1 kΩ	15	30		15	30		V/mV
		10			10			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		μV p-p
f = 10 Hz			25			25		nV/√Hz
f = 100 Hz			21			21		nV/√Hz
f = 1 kHz			16			16		nV/√Hz
f = 10 kHz			13			13		nV/√Hz
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10 kΩ to 2.5 V							
f = 10 kHz	V_O = 0.25 V to 4.75 V		–93			–93		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.8			1.8		MHz
Full Power Response	V_O p-p = 4.5 V		210			210		kHz
Slew Rate			3			3		V/μs
Settling Time								
to 0.1%	V_O = 0.2 V to 4.5 V		1.4			1.4		μs
to 0.01%			1.8			1.8		μs
INPUT CHARACTERISTICS								
Common-Mode Voltage Range[1]		–0.2		+4	–0.2		+4	V
T_{MIN} to T_{MAX}		–0.2		+4	–0.2		+4	V
CMRR	V_{CM} = 0 V to 2 V	66	80		72	80		dB
T_{MIN} to T_{MAX}		66			66			dB
Input Impedance								
Differential			10^{13}‖0.5			10^{13}‖0.5		Ω‖pF
Common Mode			10^{13}‖2.8			10^{13}‖2.8		Ω‖pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
V_{OL}–V_{EE}	I_{SINK} = 20 μA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 μA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		15			15			mA
T_{MIN} to T_{MAX}		12			12			mA
Short-Circuit Current			25			25		mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current	T_{MIN} to T_{MAX}		620	800		620	800	μA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		66	80		dB
T_{MIN} to T_{MAX}		70			66			dB

SPECIFICATIONS (V_S = 0, 5 V @ T_A = 25°C, V_{CM} = 0 V, V_{OUT} = 0.2 V unless otherwise noted.)

Parameter	Conditions	AD820A Min	AD820A Typ	AD820A Max	AD820B Min	AD820B Typ	AD820B Max	Unit
DC PERFORMANCE								
Initial Offset			0.1	0.8		0.3	0.4	mV
Max Offset over Temperature			0.5	1.5		0.5	1	mV
Offset Drift			2			2		µV/°C
Input Bias Current	V_O = –5 V to 4 V		2	25		2	10	pA
at T_{MAX}			0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
at T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_O = 4 V to –4 V							
	R_L = 100 kΩ	400	1000		400	1000		V/mV
T_{MIN} to T_{MAX}		400			400			V/mV
	R_L = 10 kΩ	80	150		80	150		V/mV
T_{MIN} to T_{MAX}		80			80			V/mV
	R_L = 1 kΩ	20	30		20	30		V/mV
T_{MIN} to T_{MAX}		10			10			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		µV p-p
f = 10 Hz			25			25		nV/√Hz
f = 100 Hz			21			21		nV/√Hz
f = 1 kHz			16			16		nV/√Hz
f = 10 kHz			13			13		nV/√Hz
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10 kΩ							
f = 10 kHz	V_O = ±4.5 V		–93			–93		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.9			1.8		MHz
Full Power Response	V_O p-p = 9 V		105			105		kHz
Slew Rate			3			3		V/µs
Settling Time								
to 0.1%	V_O = 0 V to ±4.5 V		1.4			1.4		µs
to 0.01%			1.8			1.8		µs
INPUT CHARACTERISTICS								
Common-Mode Voltage Range[1]		–5.2		+4	–5.2		+4	V
T_{MIN} to T_{MAX}		–5.2		+4	–5.2		+4	V
CMRR	V_{CM} = –5 V to +2 V	66	80		72	80		dB
T_{MIN} to T_{MAX}		66			66			dB
Input Impedance								
Differential			10^{13}‖0.5			10^{13}‖0.5		Ω‖pF
Common Mode			10^{13}‖2.8			10^{13}‖2.8		Ω‖pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
V_{OL}–V_{EE}	I_{SINK} = 20 µA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 µA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		15			15			mA
T_{MIN} to T_{MAX}		12			12			mA
Short-Circuit Current			30			30		mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current	T_{MIN} to T_{MAX}		650	800		620	800	µA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		70	80		dB
T_{MIN} to T_{MAX}		70			70			dB

AD820–SPECIFICATIONS (V_S = ±15 V @ T_A = 25°C, V_{CM} = 0 V, V_{OUT} = 0 V unless otherwise noted.)

Parameter	Conditions	AD820A Min	AD820A Typ	AD820A Max	AD820B Min	AD820B Typ	AD820B Max	Unit
DC PERFORMANCE								
Initial Offset			0.4	2		0.3	1.0	mV
Max Offset over Temperature			0.5	3		0.5	2	mV
Offset Drift			2			2		μV/°C
Input Bias Current	V_{CM} = 0 V		2	25		2	10	pA
	V_{CM} = –10 V		40			40		pA
at T_{MAX}	V_{CM} = 0 V		0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
at T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_O = +10 V to –10 V							
	R_L = 100 kΩ	500	2000		500	2000		V/mV
T_{MIN} to T_{MAX}		500			500			V/mV
	R_L = 10 kΩ	100	500		100	500		V/mV
T_{MIN} to T_{MAX}		100			100			V/mV
	R_L = 1 kΩ	30	45		30	45		V/mV
T_{MIN} to T_{MAX}		20			20			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		μV p-p
f = 10 Hz			25			25		nV/√Hz
f = 100 Hz			21			21		nV/√Hz
f = 1 kHz			16			16		nV/√Hz
f = 10 kHz			13			13		nV/√Hz
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10 kΩ							
f = 10 kHz	V_O = ±10 V		–85			–85		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.9			1.9		MHz
Full Power Response	V_O p-p = 20 V		45			45		kHz
Slew Rate			3			3		V/μs
Settling Time								
to 0.1%	V_O = 0 V to ±10 V		4.1			4.1		μs
to 0.01%			4.5			4.5		μs
INPUT CHARACTERISTICS								
Common-Mode Voltage Range[1]		–15.2		+14	–15.2		+14	V
T_{MIN} to T_{MAX}		–15.2		+14	–15.2		+14	V
CMRR	V_{CM} = –15 V to 12 V	70	80		74	90		dB
T_{MIN} to T_{MAX}		70			74			dB
Input Impedance								
Differential			10^{13}‖0.5			10^{13}‖0.5		Ω‖pF
Common Mode			10^{13}‖2.8			10^{13}‖2.8		Ω‖pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
V_{OL}–V_{EE}	I_{SINK} = 20 μA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 μA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		20			20			mA
T_{MIN} to T_{MAX}		15			15			mA
Short-Circuit Current			45			45		mA
Capacitive Load Drive			350			350		
POWER SUPPLY								
Quiescent Current	T_{MIN} to T_{MAX}		700	900		700	900	μA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		70	80		dB
T_{MIN} to T_{MAX}		70			70			dB

NOTES
[1]This is a functional specification. Amplifier bandwidth decreases when the input common-mode voltage is driven in the range ($+V_S$ – 1 V) to $+V_S$. Common-mode error voltage is typically less than 5 mV with the common-mode voltage set at 1 volt below the positive supply.
[2]V_{OL}–V_{EE} is defined as the difference between the lowest possible output voltage (V_{OL}) and the minus voltage supply rail (V_{EE}). V_{CC}–V_{OH} is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation[2]
  Plastic DIP (N) . . . . 1.6 W
  SOIC (R) . . . . 1.0 W
Input Voltage . . . . ($+V_S$ + 0.2 V) to – (20 V + V_S)
Output Short Circuit Duration . . . . Indefinite
Differential Input Voltage . . . . ±30 V
Storage Temperature Range (N) . . . . –65°C to +125°C
Storage Temperature Range (R) . . . . –65°C to +150°C
Operating Temperature Range
  AD820A/B . . . . –40°C to +85°C
Lead Temperature Range
  (Soldering 60 sec) . . . . 260°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Lead Plastic DIP Package: θ_{JA} = 90°C/W
8-Lead SOIC Package: θ_{JA} = 160°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD820AN	–40°C to +85°C	8-Lead Plastic Mini-DIP	N-8
AD820BN*	–40°C to +85°C	8-Lead Plastic Mini-DIP	N-8
AD820AR	–40°C to +85°C	8-Lead SOIC	R-8
AD820BR	–40°C to +85°C	8-Lead SOIC	R-8

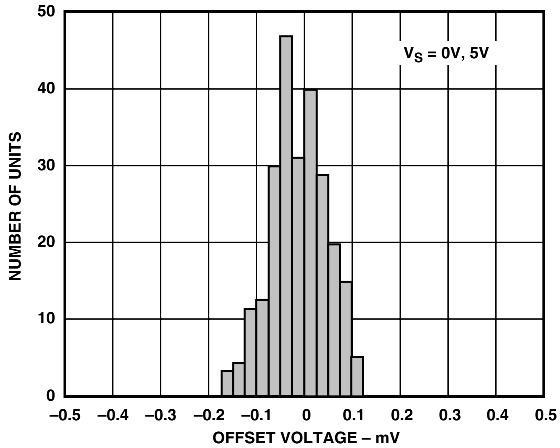
*Not for new design, obsolete April 2002.

CAUTION

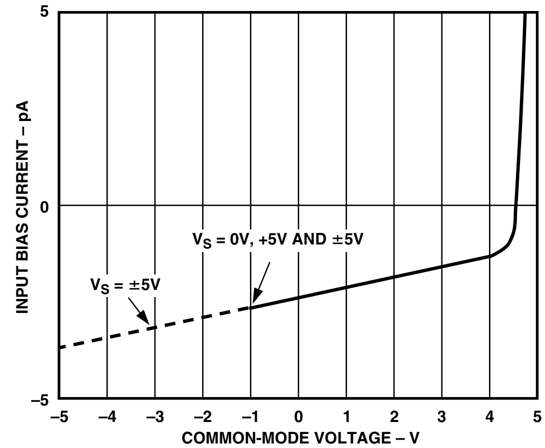
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD820 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



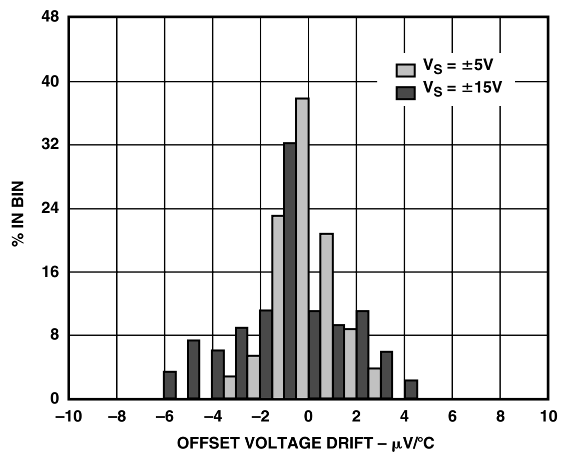
AD820–Typical Performance Characteristics



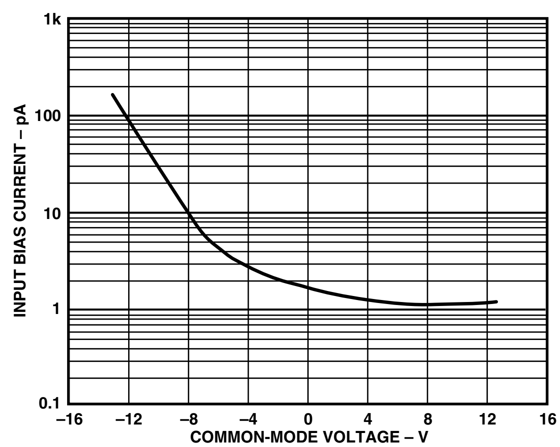
TPC 1. Typical Distribution of Offset Voltage (248 Units)



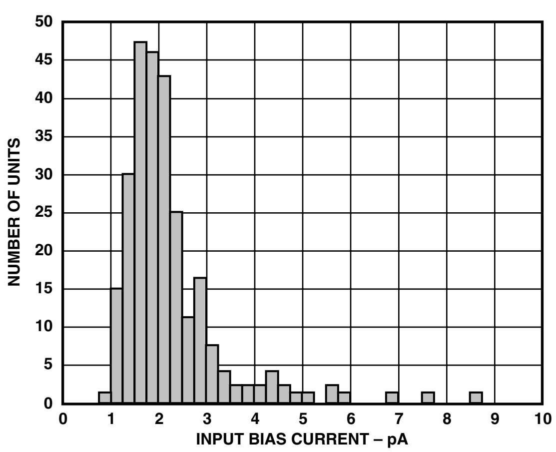
TPC 4. Input Bias Current vs. Common-Mode Voltage; V_S = +5 V, 0 V and V_S = ±5 V



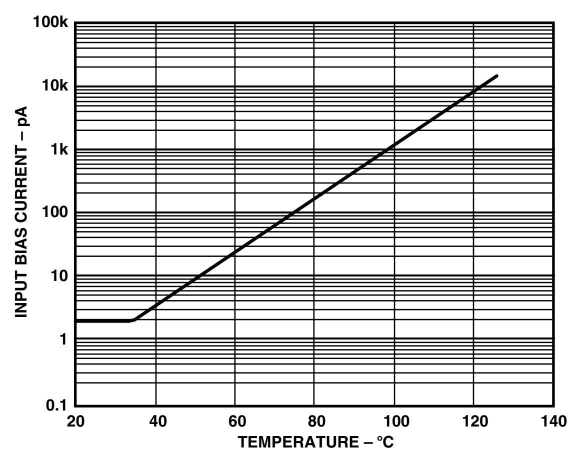
TPC 2. Typical Distribution of Offset Voltage Drift (120 Units)



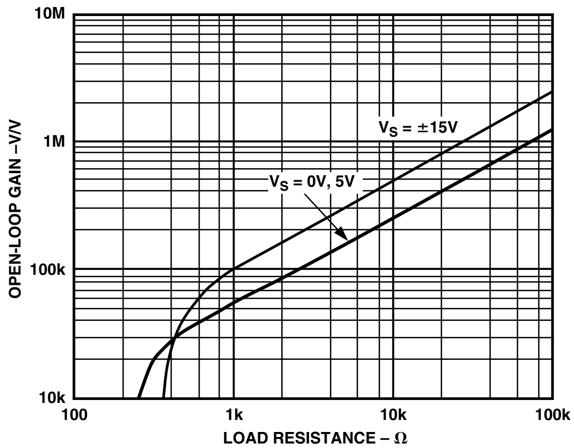
TPC 5. Input Bias Current vs. Common-Mode Voltage; V_S = ±15 V



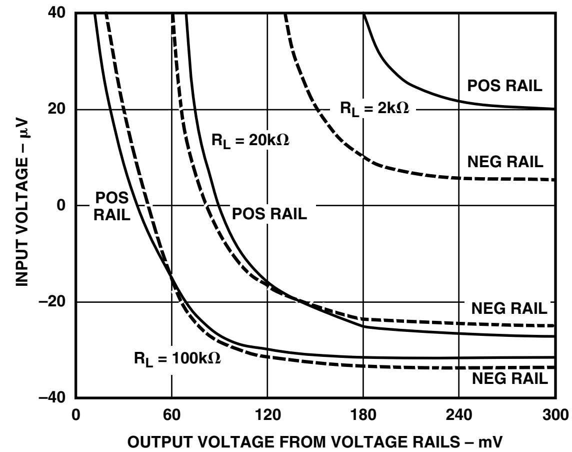
TPC 3. Typical Distribution of Input Bias Current (213 Units)



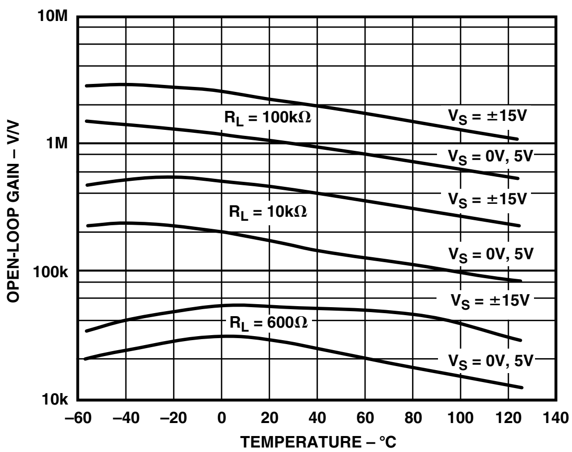
TPC 6. Input Bias Current vs. Temperature; V_S = 5 V, V_{CM} = 0



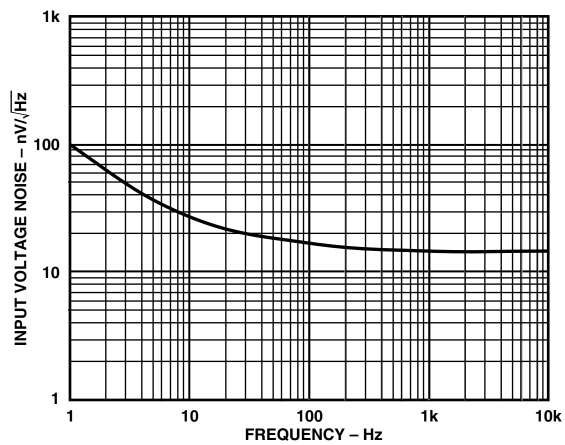
TPC 7. Open-Loop Gain vs. Load Resistance



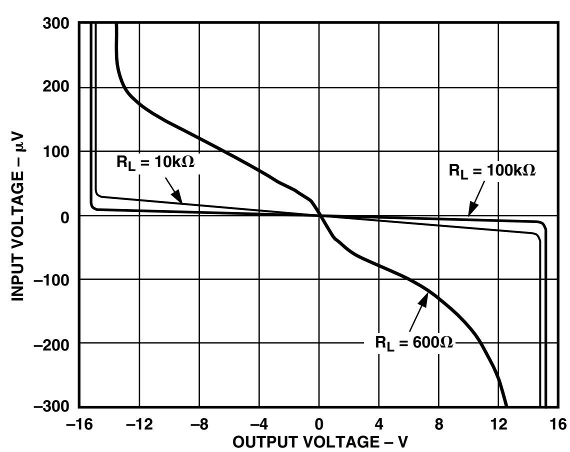
TPC 10. Input Error Voltage with Output Voltage within 300 mV of Either Supply Rail for Various Resistive Loads; $V_S = \pm5$ V



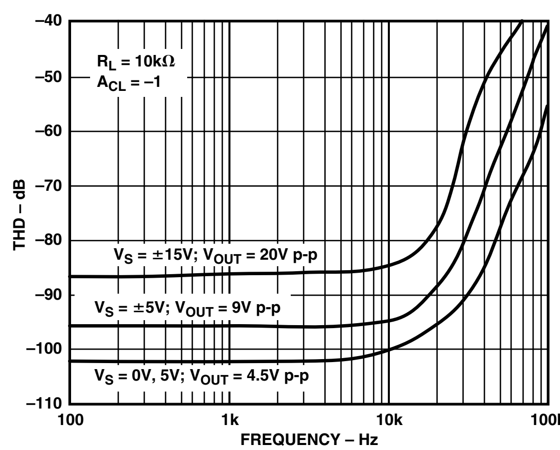
TPC 8. Open-Loop Gain vs. Temperature



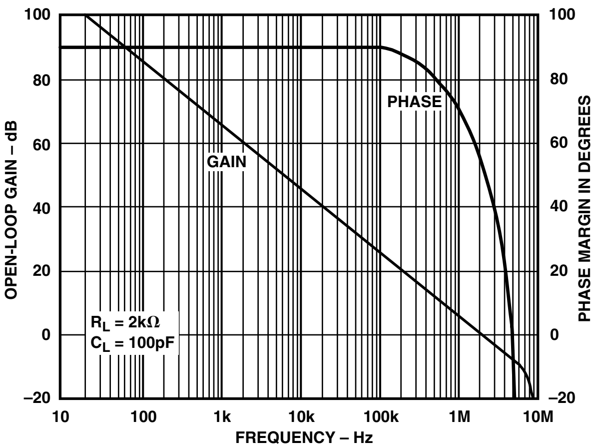
TPC 11. Input Voltage Noise vs. Frequency



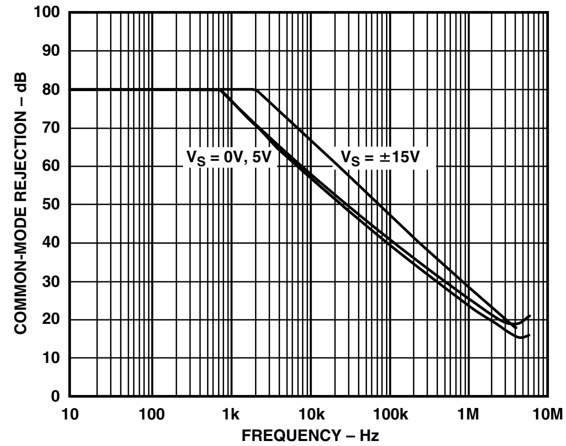
TPC 9. Input Error Voltage vs. Output Voltage for Resistive Loads



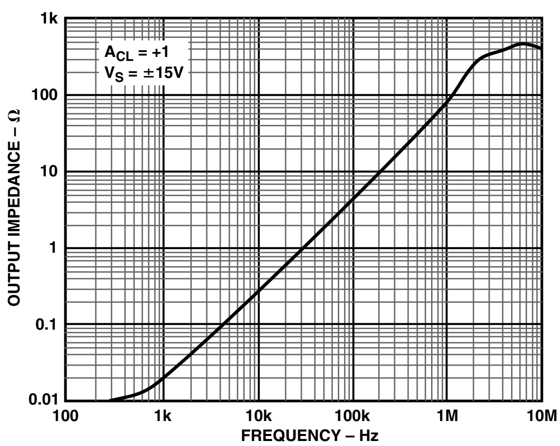
TPC 12. Total Harmonic Distortion vs. Frequency



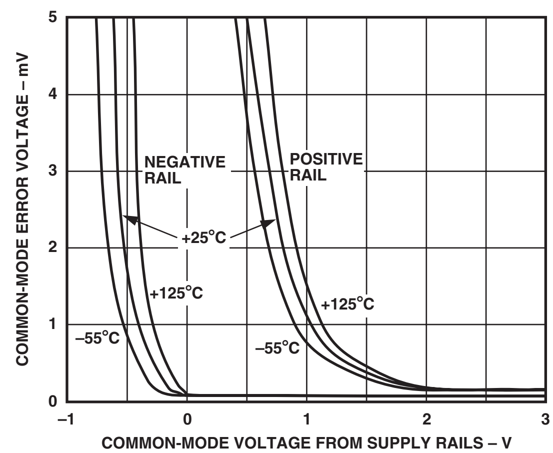
TPC 13. Open-Loop Gain and Phase Margin vs. Frequency



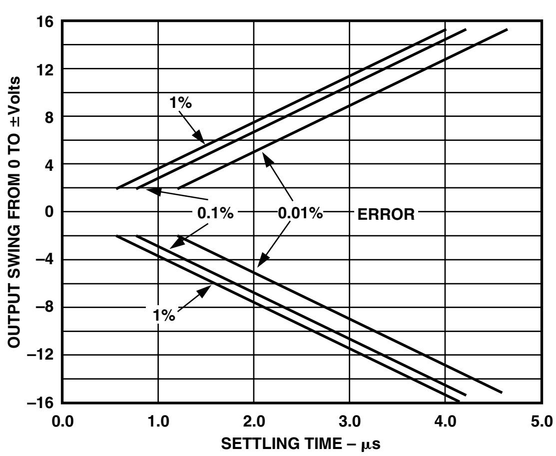
TPC 16. Common-Mode Rejection vs. Frequency



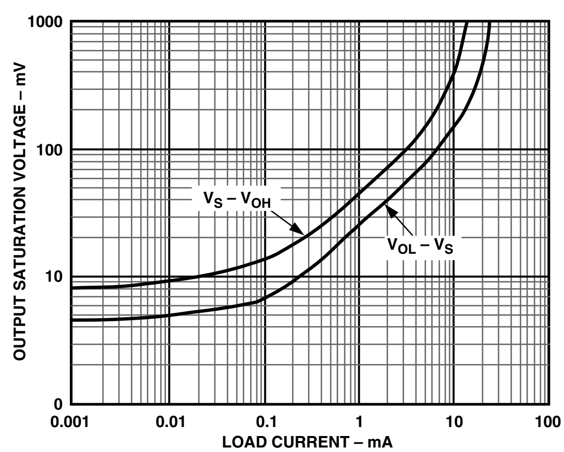
TPC 14. Output Impedance vs. Frequency



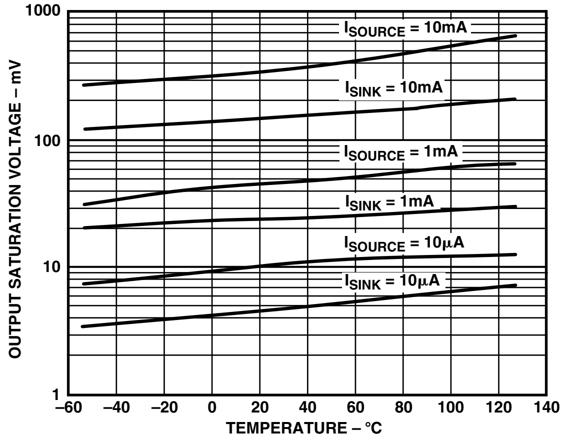
TPC 17. Absolute Common-Mode Error vs. Common-Mode Voltage from Supply Rails (V_S – V_{CM})



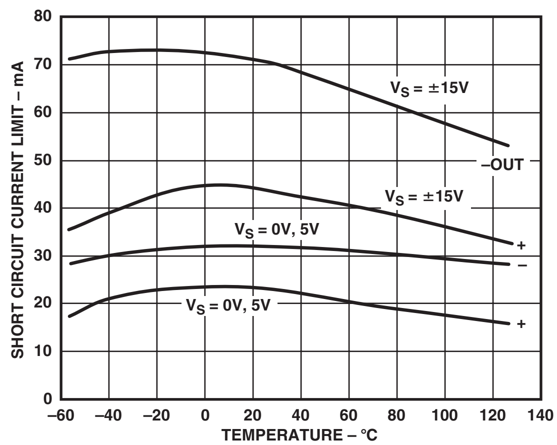
TPC 15. Output Swing and Error vs. Settling Time



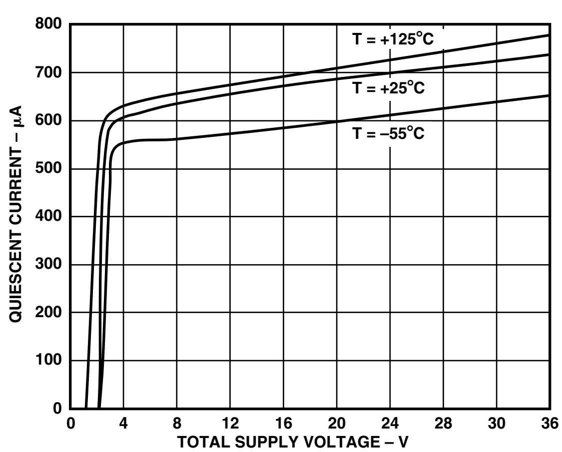
TPC 18. Output Saturation Voltage vs. Load Current



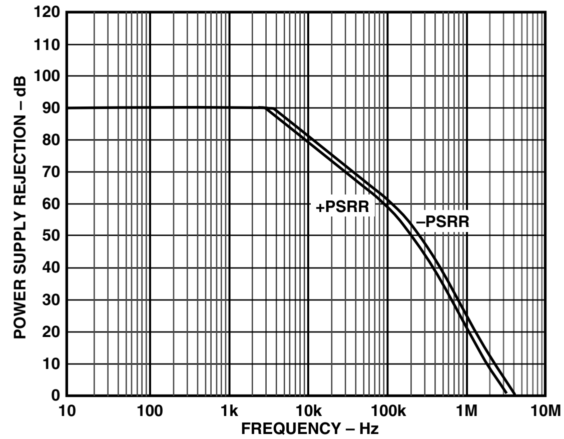
TPC 19. Output Saturation Voltage vs. Temperature



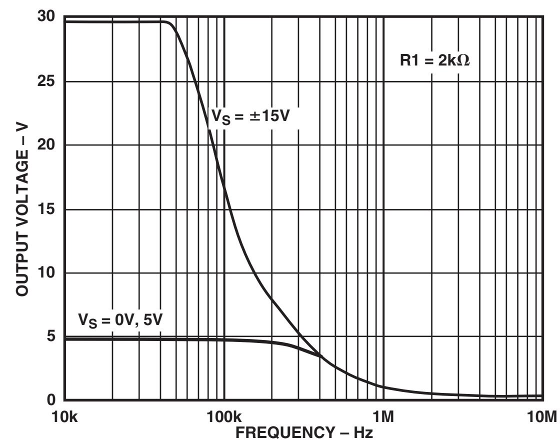
TPC 20. Short Circuit Current Limit vs. Temperature



TPC 21. Quiescent Current vs. Supply Voltage vs. Temperature



TPC 22. Power Supply Rejection vs. Frequency



TPC 23. Large Signal Frequency Response

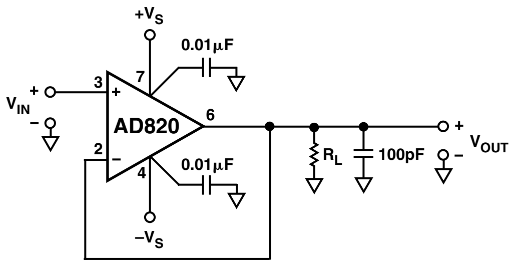


Figure 3. Unity Gain Follower

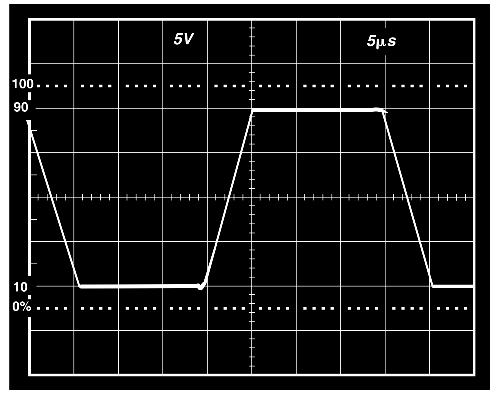


Figure 6. Large Signal Response Unity Gain Follower; $V_S = \pm 15$ V, $R_L = 10$ kΩ

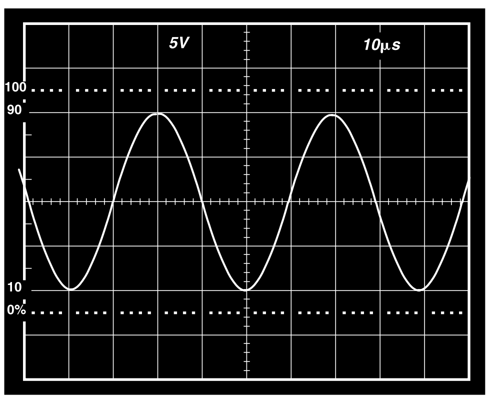


Figure 4. 20 V, 25 kHz Sine Input; Unity Gain Follower; $R_L = 600$ Ω, $V_S = \pm 15$ V

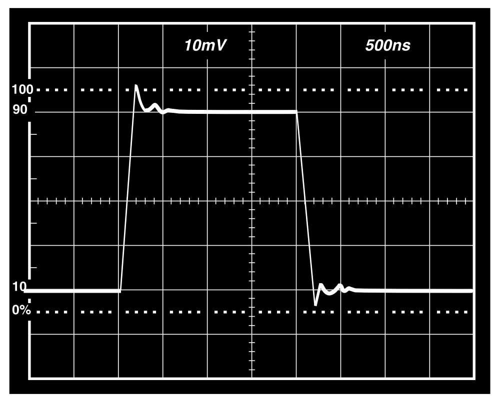


Figure 7. Small Signal Response Unity Gain Follower; $V_S = \pm 15$ V, $R_L = 10$ kΩ

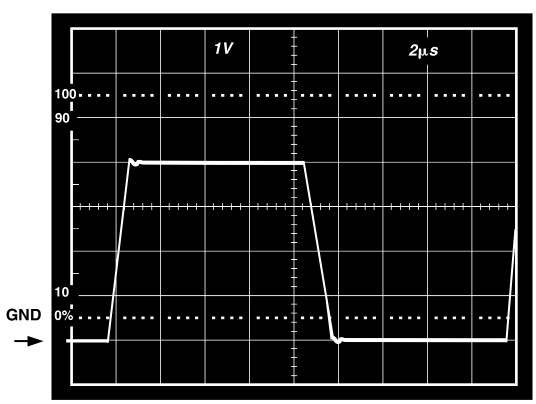


Figure 5. $V_S = 5$ V, 0 V; Unity Gain Follower Response to 0 V to 4 V Step

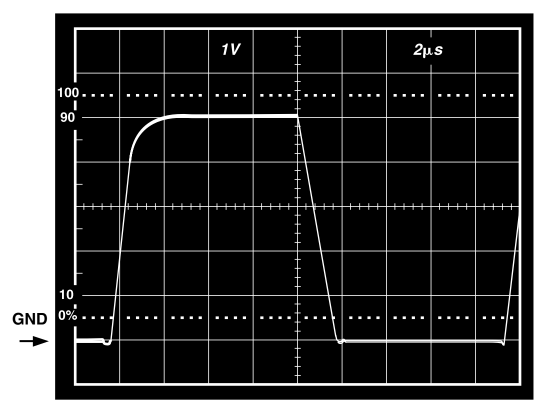


Figure 8. $V_S = 5$ V, 0 V; Unity Gain Follower Response to 0 V to 5 V Step

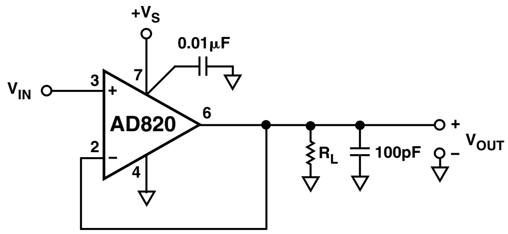


Figure 9. Unity Gain Follower

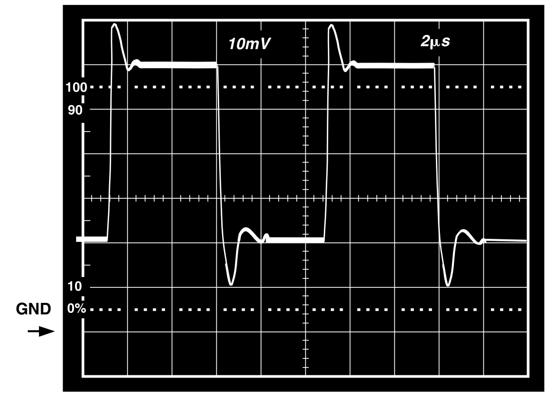


Figure 12. V_S = 5 V, 0 V; Unity Gain Follower Response to 40 mV Step Centered 40 mV above Ground

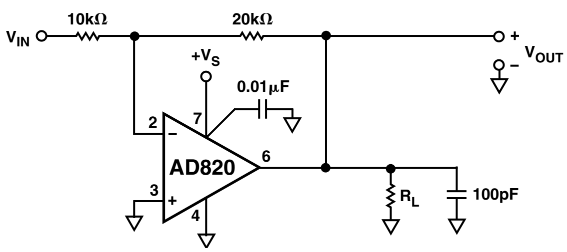


Figure 10. Gain of Two Inverter

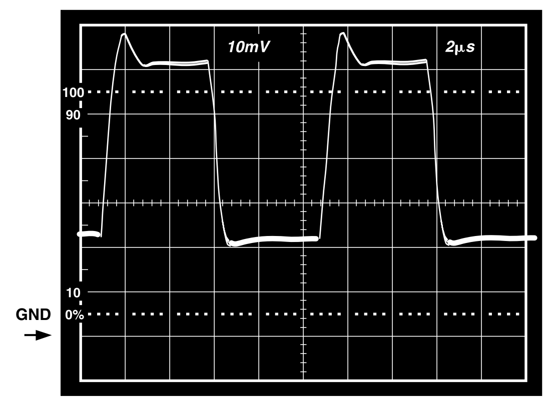


Figure 13. V_S = 5 V, 0 V; Gain-of-Two Inverter Response to 20 mV Step, Centered 20 mV below Ground

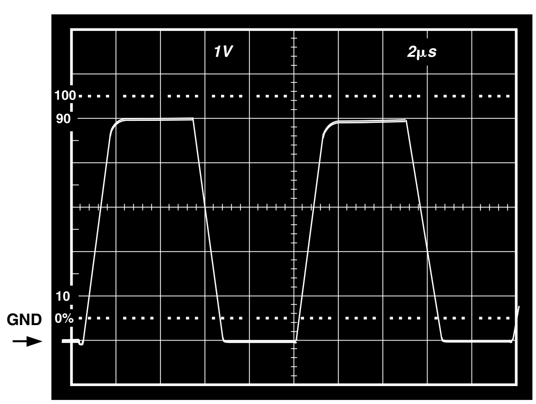


Figure 11. V_S = 5 V, 0 V; Gain-of-Two Inverter Response to 2.5 V Step Centered –1.25 V below Ground

APPLICATION NOTES

Input Characteristics

In the AD820, n-channel JFETs are used to provide a low offset, low noise, high impedance input stage. Minimum input common-mode voltage extends from 0.2 V below $-V_S$ to 1 V less than $+V_S$. Driving the input voltage closer to the positive rail will cause a loss of amplifier bandwidth (as can be seen by comparing the large signal responses shown in Figures 5 and 8) and increased common-mode voltage error as illustrated in TPC 11.

The AD820 does not exhibit phase reversal for input voltages up to and including $+V_S$. Figure 14a shows the response of an AD820 voltage follower to a 0 V to 5 V ($+V_S$) square wave input. The input and output are superimposed. The output polarity tracks the input polarity up to $+V_S$—no phase reversal. The reduced bandwidth above a 4 V input causes the rounding of the output wave form. For input voltages greater than $+V_S$, a resistor in series with the AD820's plus input will prevent phase reversal, at the expense of greater input voltage noise. This is illustrated in Figure 14b.

Since the input stage uses n-channel JFETs, input current during normal operation is negative; the current flows out from the input terminals. If the input voltage is driven more positive than $+V_S$ – 0.4 V, the input current will reverse direction as internal device junctions become forward biased. This is illustrated in TPC 4.

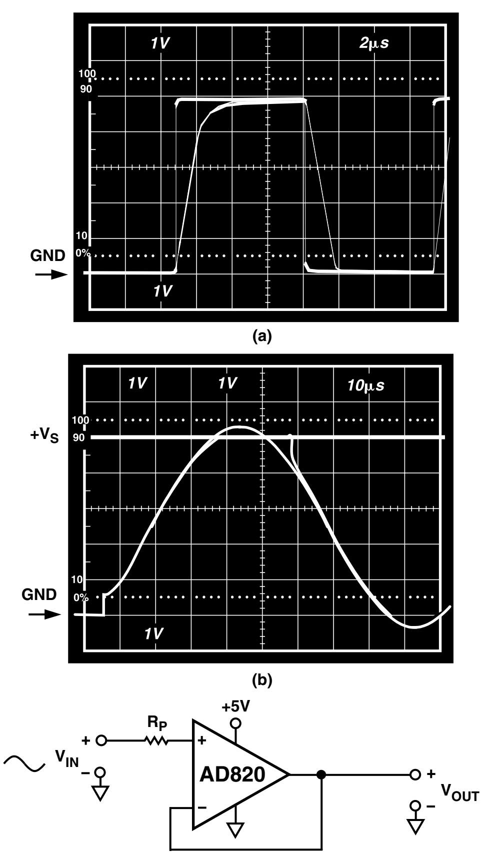


Figure 14. (a) Response with $R_P = 0$; V_{IN} from 0 to $+V_S$
(b) $V_{IN} = 0$ to $+V_S + 200$ mV
$V_{OUT} = 0$ to $+V_S$
$R_P = 49.9$ kΩ

A current limiting resistor should be used in series with the input of the AD820 if there is a possibility of the input voltage exceeding the positive supply by more than 300 mV, or if an input voltage will be applied to the AD820 when $\pm V_S = 0$. The amplifier will be damaged if left in that condition for more than 10 seconds. A 1 kΩ resistor allows the amplifier to withstand up to 10 volts of continuous overvoltage, and increases the input voltage noise by a negligible amount.

Input voltages less than $-V_S$ are a completely different story. The amplifier can safely withstand input voltages 20 V below the minus supply voltage as long as the total voltage from the positive supply to the input terminal is less than 36 V. In addition, the input stage typically maintains picoamp level input currents across that input voltage range.

The AD820 is designed for 13 nV/$\sqrt{Hz}$ wideband input voltage noise and maintains low noise performance to low frequencies (refer to TPC 11). This noise performance, along with the AD820's low input current and current noise means that the AD820 contributes negligible noise for applications with source resistances greater than 10 kΩ and signal bandwidths greater than 1 kHz. This is illustrated in Figure 15.

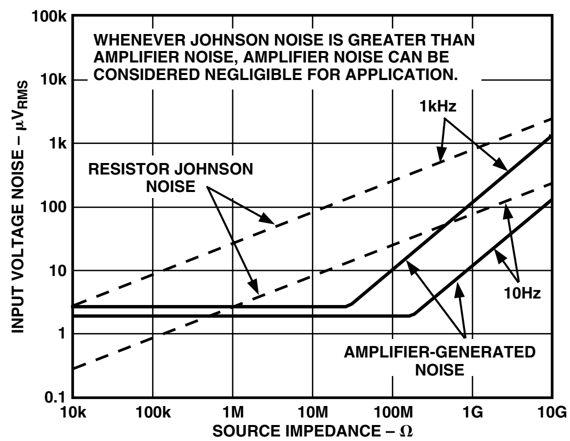


Figure 15. Total Noise vs. Source Impedance

Output Characteristics

The AD820's unique bipolar rail-to-rail output stage swings within 5 mV of the minus supply and 10 mV of the positive supply with no external resistive load. The AD820's approximate output saturation resistance is 40 Ω sourcing and 20 Ω sinking. This can be used to estimate output saturation voltage when driving heavier current loads. For instance, when sourcing 5 mA, the saturation voltage to the positive supply rail will be 200 mV, when sinking 5 mA, the saturation voltage to the minus rail will be 100 mV.

The amplifier's open-loop gain characteristic will change as a function of resistive load, as shown in TPCs 7 through 10. For load resistances over 20 kΩ, the AD820's input error voltage is virtually unchanged until the output voltage is driven to 180 mV of either supply.

If the AD820's output is driven hard against the output saturation voltage, it will recover within 2 µs of the input returning to the amplifier's linear operating region.

Direct capacitive load will interact with the amplifier's effective output impedance to form an additional pole in the amplifier's feedback loop, which can cause excessive peaking on the pulse response or loss of stability. Worst case is when the amplifier is used as a unity gain follower. Figure 16 shows the AD820's pulse response as a unity gain follower driving 350 pF. This amount of overshoot indicates approximately 20 degrees of phase margin—the system is stable, but is nearing the edge. Configurations with less loop gain, and as a result less loop bandwidth, will be much less sensitive to capacitance load effects. Figure 17 is a plot of capacitive load that will result in a 20 degree phase margin versus noise gain for the AD820. Noise gain is the inverse of the feedback attenuation factor provided by the feedback network in use.

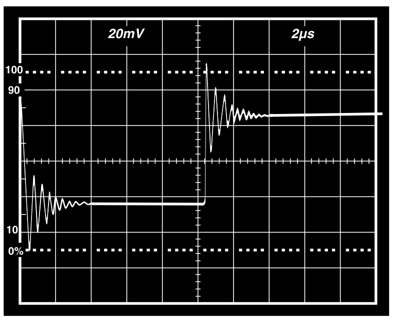


Figure 16. Small Signal Response of AD820 as Unity Gain Follower Driving 350 pF Capacitive Load

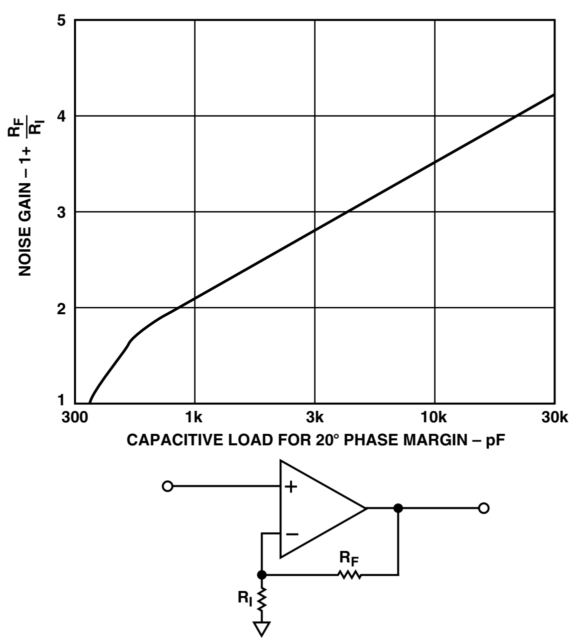


Figure 17. Capacitive Load Tolerance vs. Noise Gain

Figure 18 shows a possible configuration for extending capacitance load drive capability for a unity gain follower. With these component values, the circuit will drive 5,000 pF with a 10% overshoot.

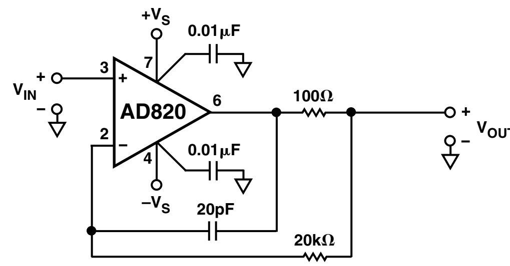


Figure 18. Extending Unity Gain Follower Capacitive Load Capability Beyond 350 pF

OFFSET VOLTAGE ADJUSTMENT

The AD820's offset voltage is low, so external offset voltage nulling is not usually required. Figure 19 shows the recommended technique for AD820's packaged in plastic DIPs. Adjusting offset voltage in this manner will change the offset voltage temperature drift by 4 μV/°C for every millivolt of induced offset. The null pins are not functional for AD820s in the SO-8 "R" package.

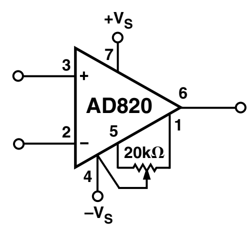


Figure 19. Offset Null

APPLICATIONS

Single Supply Half-Wave and Full-Wave Rectifiers

An AD820 configured as a unity gain follower and operated with a single supply can be used as a simple half-wave rectifier. The AD820's inputs maintain picoamp level input currents even when driven well below the minus supply. The rectifier puts that behavior to good use, maintaining an input impedance of over 10^{11} Ω for input voltages from 1 volt from the positive supply to 20 volts below the negative supply.

The full and half-wave rectifier shown in Figure 20 operates as follows: when V_{IN} is above ground, R1 is bootstrapped through the unity gain follower A1 and the loop of amplifier A2. This forces the inputs of A2 to be equal, thus no current flows through R1 or R2, and the circuit output tracks the input. When V_{IN} is below ground, the output of A1 is forced to ground. The noninverting input of amplifier A2 sees the ground level output of A1, therefore, A2 operates as a unity gain inverter. The output at node C is then a full-wave rectified version of the input. Node B is a buffered half-wave rectified version of the input. Input voltages up to ±18 volts can be rectified, depending on the voltage supply used.

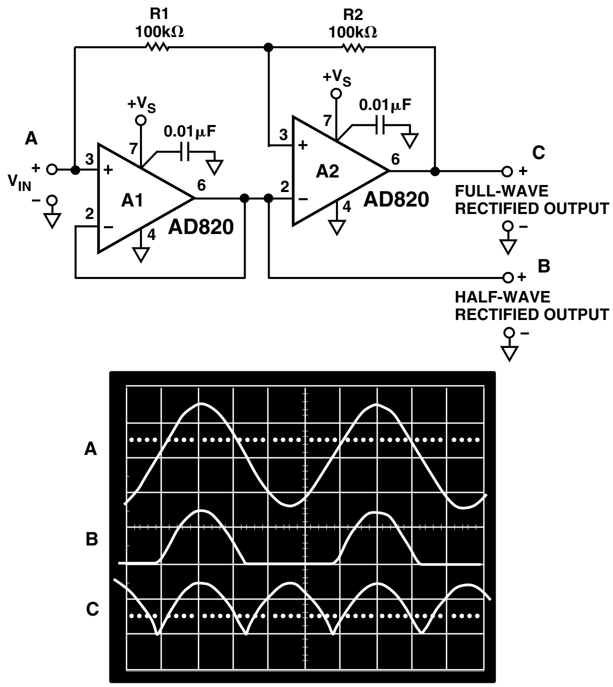


Figure 20. Single Supply Half- and Full-Wave Rectifier

4.5 V Low Dropout, Low Power Reference

The rail-to-rail performance of the AD820 can be used to provide low dropout performance for low power reference circuits powered with a single low voltage supply. Figure 21 shows a 4.5 V reference using the AD820 and the AD680, a low power 2.5 V bandgap reference. R2 and R3 set up the required gain of 1.8 to develop the 4.5 V output. R1 and C2 form a low-pass RC filter to reduce the noise contribution of the AD680.

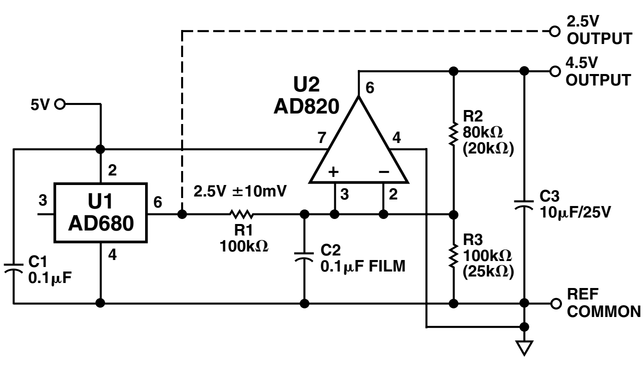


Figure 21. Single Supply 4.5 V Low Dropout Reference

With a 1 mA load, this reference maintains the 4.5 V output with a supply voltage down to 4.7 V. The amplitude of the recovery transient for a 1 mA to 10 mA step change in load current is under 20 mV, and settles out in a few microseconds. Output voltage noise is less than 10 μV rms in a 25 kHz noise bandwidth.

Low Power Three-Pole Sallen Key Low-Pass Filter

The AD820's high input impedance makes it a good selection for active filters. High value resistors can be used to construct low frequency filters with capacitors much less than 1 μF. The AD820's picoamp level input currents contribute minimal dc errors.

Figure 22 shows an example, a 10 Hz three-pole Sallen Key Filter. The high value used for R1 minimizes interaction with signal source resistance. Pole placement in this version of the filter minimizes the Q associated with the two-pole section of the filter. This eliminates any peaking of the noise contribution of resistors R1, R2, and R3, thus minimizing the inherent output voltage noise of the filter.

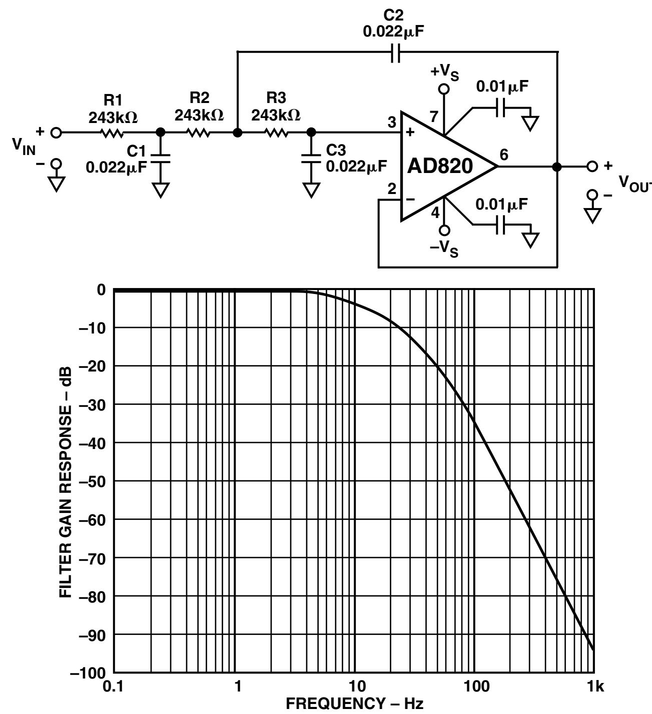
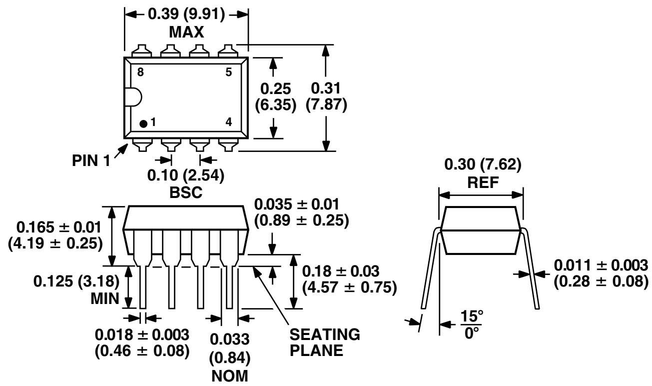


Figure 22. 10 Hz Sallen Key Low-Pass Filter

OUTLINE DIMENSIONS

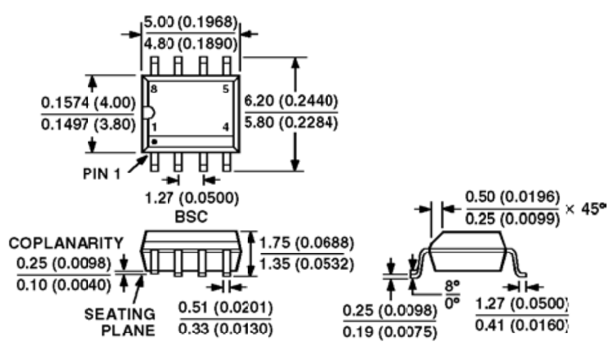
Mini-DIP Package
(N-8)

Dimensions shown in inches and (millimeters)



SOIC Package
(R-8)

Dimensions shown in millimeters (inches)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

COMPLIANT TO JEDEC STANDARDS MS-012 AA

Revision History

Location	Page
Data Sheet changed from REV. C to REV. D.	
Changeto SOIC Package (R-8) Drawing	15
Edits to FEATURES	1
Edits to PRODUCT DESCRIPTION	1
Delete SPECIFICATIONS for AD820A-3 V	5
Edits to ORDERING GUIDE	6
Edits to TYPICAL PERFORMANCE CHARACTERISTICS	8

C00873–0–5/02(D)

PRINTED IN U.S.A.

November 1999

National Semiconductor

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit µP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

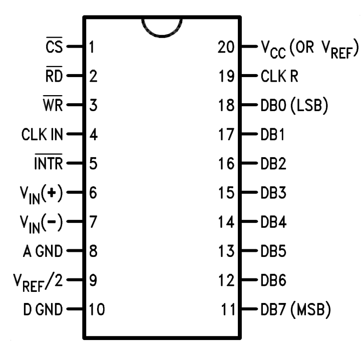
- Compatible with 8080 µP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

- Resolution: 8 bits
- Total error: ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time: 100 µs

Connection Diagram

ADC080X
Dual-In-Line and Small Outline (SO) Packages



DS005671-30

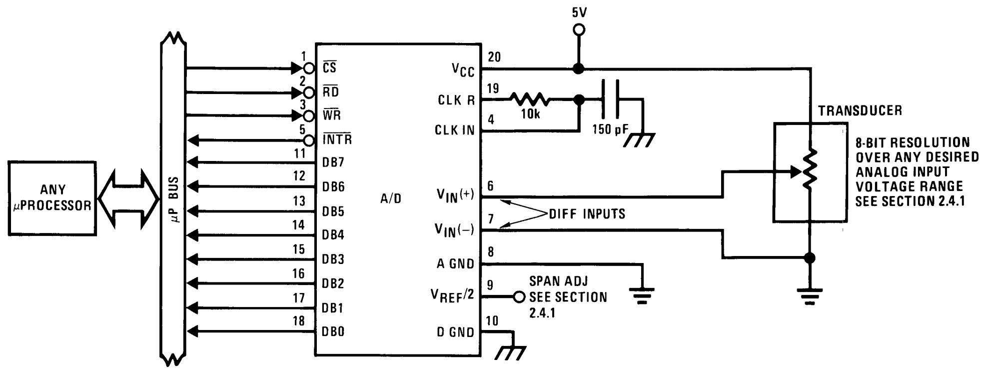
See Ordering Information

Ordering Information

TEMP RANGE		0˚C TO 70˚C	0˚C TO 70˚C	−40˚C TO +85˚C
ERROR	±¼ Bit Adjusted			ADC0801LCN
	±½ Bit Unadjusted	ADC0802LCWM		ADC0802LCN
	±½ Bit Adjusted			ADC0803LCN
	±1Bit Unadjusted	ADC0804LCWM	ADC0804LCN	ADC0805LCN/ADC0804LCJ
PACKAGE OUTLINE		M20B—Small Outline	N20A—Molded DIP	

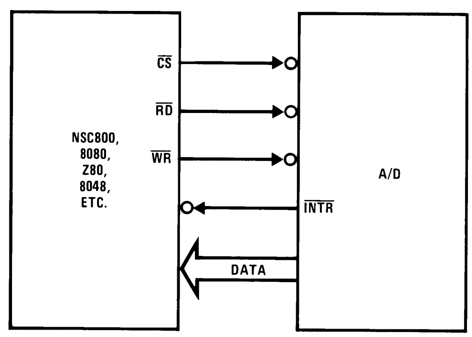
Z-80® is a registered trademark of Zilog Corp.

Typical Applications



DS005671-1

8080 Interface



DS005671-31

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	**Full-Scale Adjusted**	**V_{REF}/2=2.500 V_{DC} (No Adjustments)**	**V_{REF}/2=No Connection (No Adjustments)**
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC}+0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260˚C
Dual-In-Line Package (ceramic)	300˚C
Surface Mount Package	
Vapor Phase (60 seconds)	215˚C
Infrared (15 seconds)	220˚C
Storage Temperature Range	−65˚C to +150˚C
Package Dissipation at T_A=25˚C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0804LCJ	−40˚C≤T_A≤+85˚C
ADC0801/02/03/05LCN	−40˚C≤T_A≤+85˚C
ADC0804LCN	0˚C≤T_A≤+70˚C
ADC0802/04LCWM	0˚C≤T_A≤+70˚C
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	V_{REF}/2=2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	V_{REF}/2=2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	V_{REF}/2-No Connection			±1	LSB
V_{REF}/2 Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd–0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC}=5 V_{DC} ±10% Over Allowed V_{IN}(+) and V_{IN}(−) Voltage Range (Note 4)		±1/16	±⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK}=640 kHz (Note 6)	103		114	µs
T_C	Conversion Time	(Notes 5, 6)	66		73	1/f_{CLK}
f_{CLK}	Clock Frequency Clock Duty Cycle	V_{CC}=5V, (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ =0 V_{DC}, f_{CLK}=640 kHz	8770		9708	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ =0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L=100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC}=5 V_{DC} and T_{MIN}≤T_A≤T_{MAX} unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical “1” Input Voltage (Except Pin 4 CLK IN)	V_{CC}=5.25 V_{DC}	2.0		15	V_{DC}
V_{IN} (0)	Logical “0” Input Voltage (Except Pin 4 CLK IN)	V_{CC}=4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical “1” Input Current (All Inputs)	V_{IN}=5 V_{DC}		0.005	1	µA_{DC}
I_{IN} (0)	Logical “0” Input Current (All Inputs)	V_{IN}=0 V_{DC}	−1	−0.005		µA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T−	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis (V_T+)−(V_T−)		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical “0” CLK R Output Voltage	I_O=360 µA V_{CC}=4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical “1” CLK R Output Voltage	I_O=−360 µA V_{CC}=4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical “0” Output Voltage					
	Data Outputs	I_{OUT}=1.6 mA, V_{CC}=4.75 V_{DC}			0.4	V_{DC}
	$\overline{INTR}$ Output	I_{OUT}=1.0 mA, V_{CC}=4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical “1” Output Voltage	I_O=−360 µA, V_{CC}=4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical “1” Output Voltage	I_O=−10 µA, V_{CC}=4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT}=0 V_{DC}	−3			µA_{DC}
		V_{OUT}=5 V_{DC}			3	µA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A=25˚C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A=25˚C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current)	f_{CLK}=640 kHz, V_{REF}/2=NC, T_A=25˚C and $\overline{CS}$ =5V				
	ADC0801/02/03/04LCJ/05			1.1	1.8	mA
	ADC0804LCN/LCWM			1.9	2.5	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For V_{IN}(−)≥ V_{IN}(+) the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct–especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 4* and section 2.0.

AC Electrical Characteristics (Continued)

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

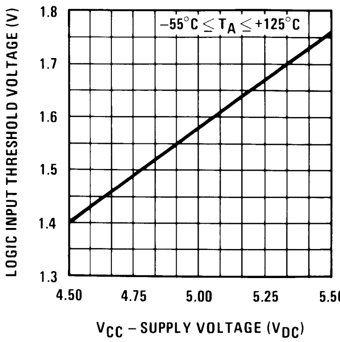
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 7*.

Note 9: The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

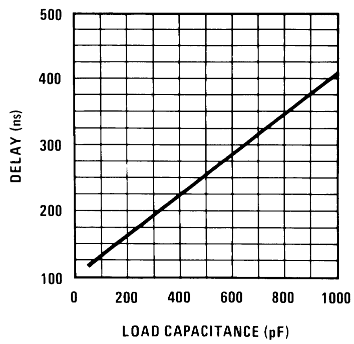
Typical Performance Characteristics

Logic Input Threshold Voltage vs. Supply Voltage



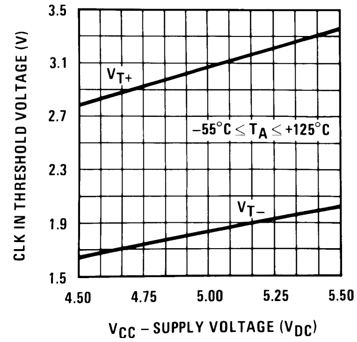
DS005671-38

Delay From Falling Edge of RD to Output Data Valid vs. Load Capacitance



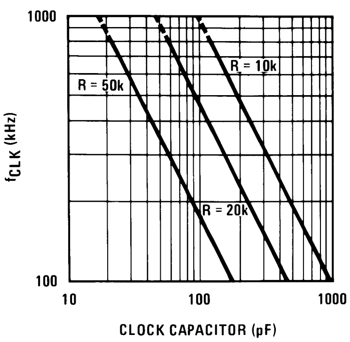
DS005671-39

CLK IN Schmitt Trip Levels vs. Supply Voltage



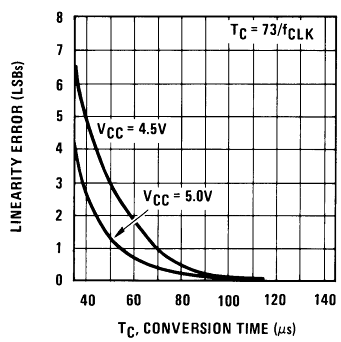
DS005671-40

f_{CLK} vs. Clock Capacitor



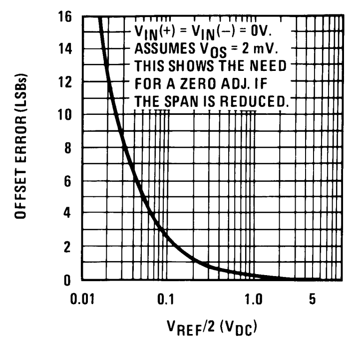
DS005671-41

Full-Scale Error vs Conversion Time



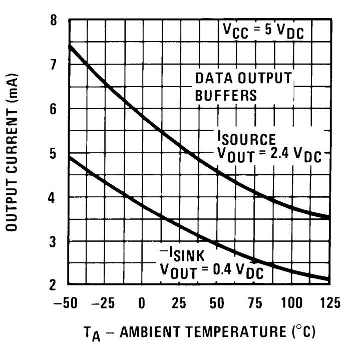
DS005671-42

Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



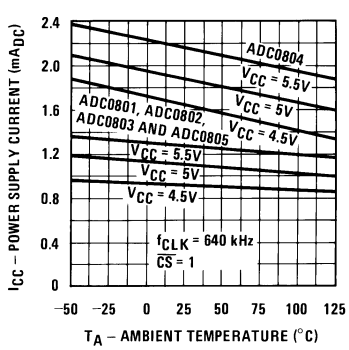
DS005671-43

Output Current vs Temperature



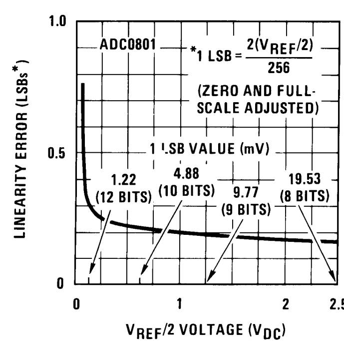
DS005671-44

Power Supply Current vs Temperature (Note 9)



DS005671-45

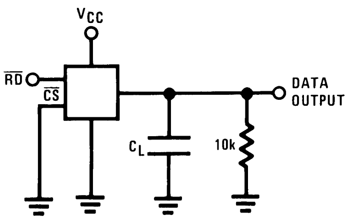
Linearity Error at Low $V_{REF}/2$ Voltages



DS005671-46

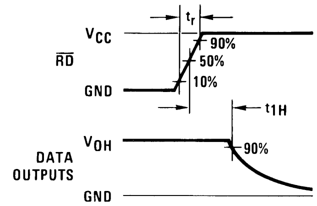
TRI-STATE Test Circuits and Waveforms

t_{1H}



DS005671-47

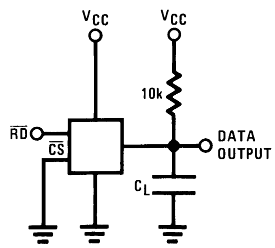
t_{1H}, C_L=10 pF



DS005671-48

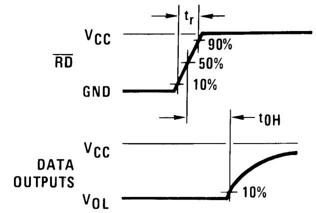
t_r=20 ns

t_{0H}



DS005671-49

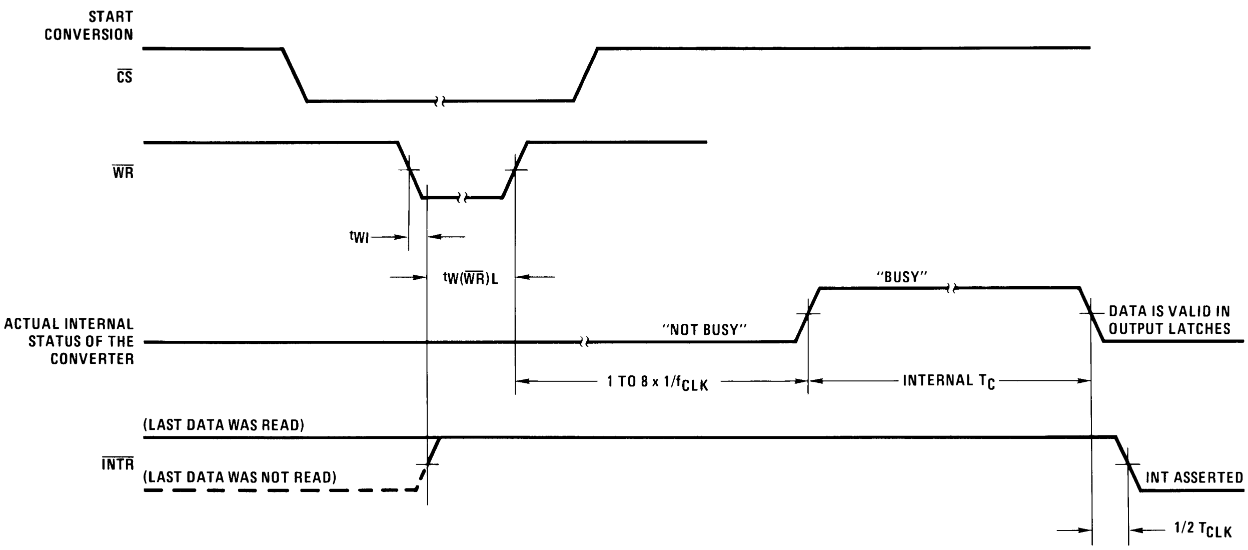
t_{0H}, C_L=10 pF



DS005671-50

t_r=20 ns

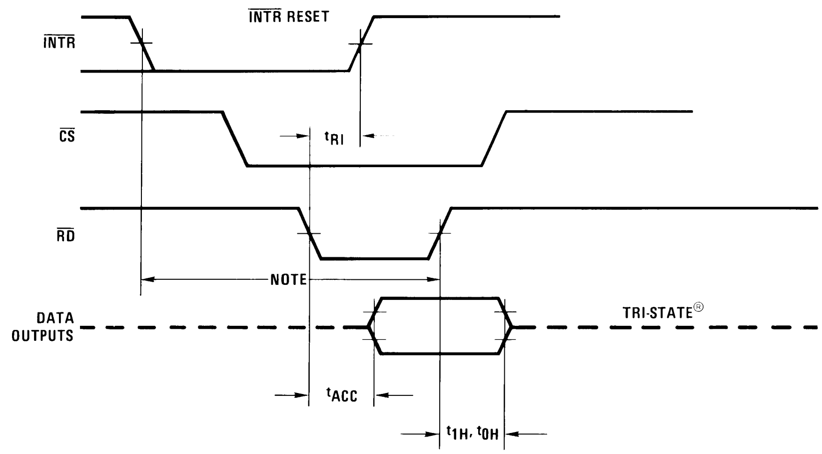
Timing Diagrams (All timing is measured from the 50% voltage points)



DS005671-51

Timing Diagrams (All timing is measured from the 50% voltage points) (Continued)

Output Enable and Reset with $\overline{INTR}$

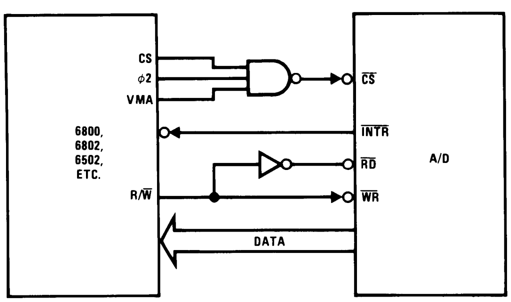


DS005671-52

Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

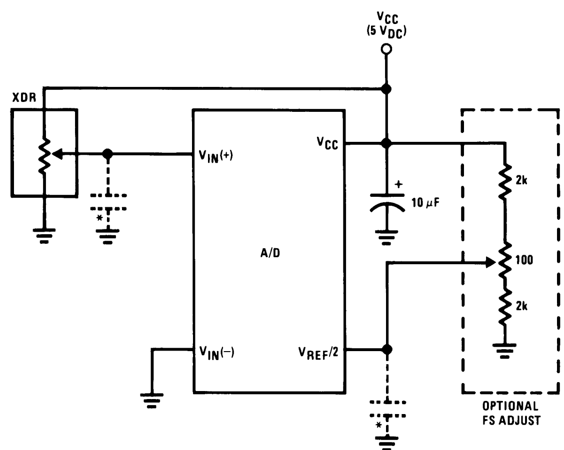
Typical Applications

6800 Interface



DS005671-53

Ratiometeric with Full-Scale Adjust

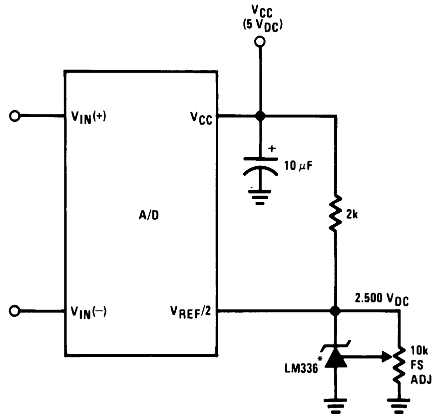


DS005671-54

Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

Typical Applications (Continued)

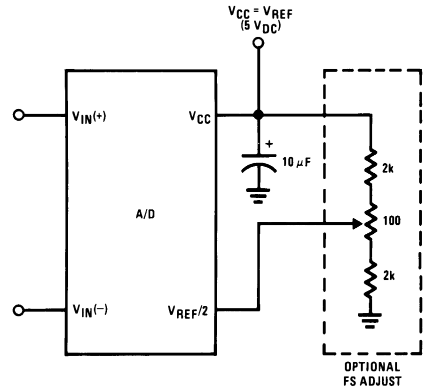
Absolute with a 2.500V Reference



DS005671-55

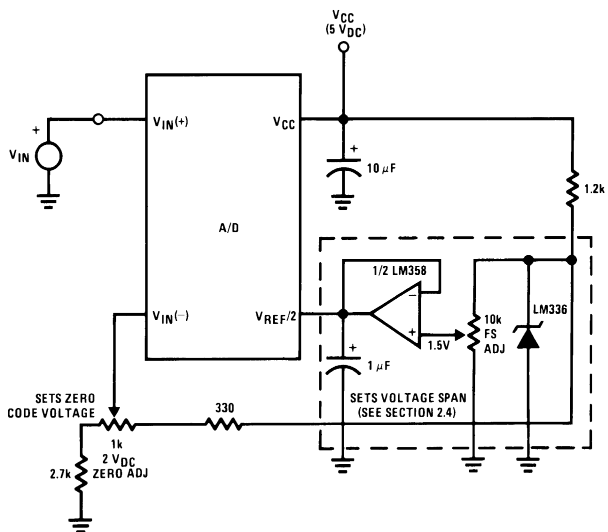
*For low power, see also LM385–2.5

Absolute with a 5V Reference



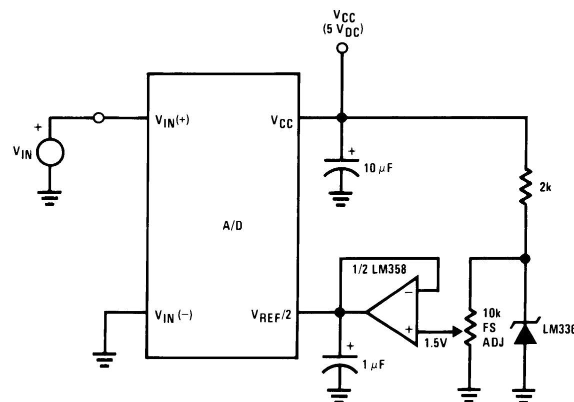
DS005671-56

Zero-Shift and Span Adjust: 2V ≤ V_{IN} ≤ 5V



DS005671-57

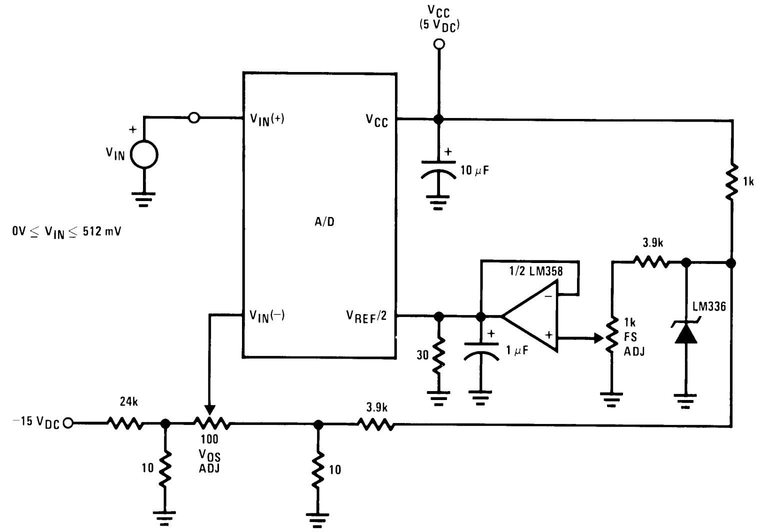
Span Adjust: 0V ≤ V_{IN} ≤ 3V



DS005671-58

Typical Applications (Continued)

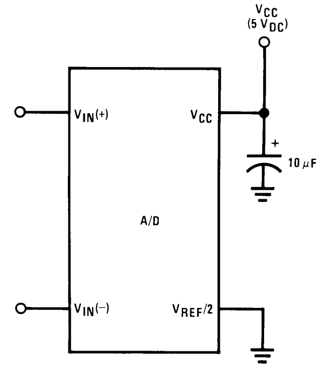
Directly Converting a Low-Level Signal



DS005671-59

$V_{REF}/2$=256 mV

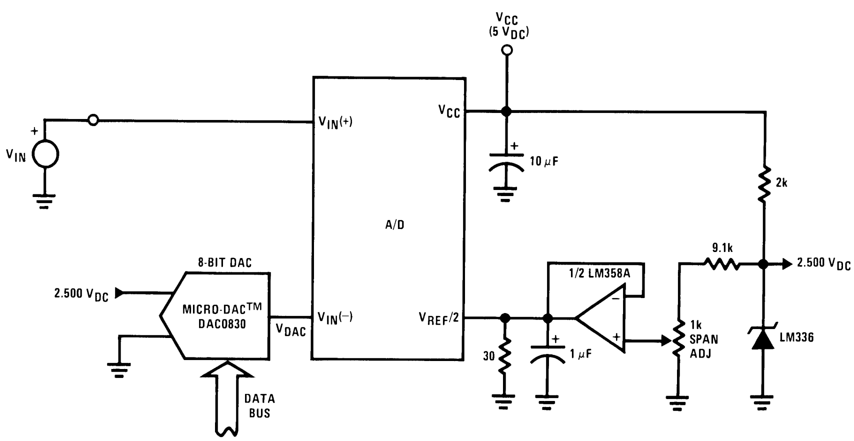
A µP Interfaced Comparator



DS005671-60

For:
$V_{IN}(+) > V_{IN}(-)$
Output=FF_{HEX}
For:
$V_{IN}(+) < V_{IN}(-)$
Output=00_{HEX}

1 mV Resolution with µP Controlled Range

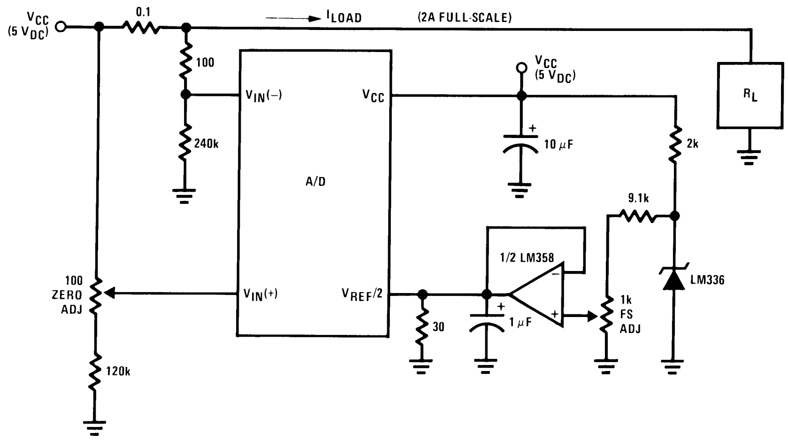


DS005671-61

$V_{REF}/2$=128 mV
1 LSB=1 mV
$V_{DAC} \leq V_{IN} \leq (V_{DAC}+256\text{ mV})$
$0 \leq V_{DAC} < 2.5V$

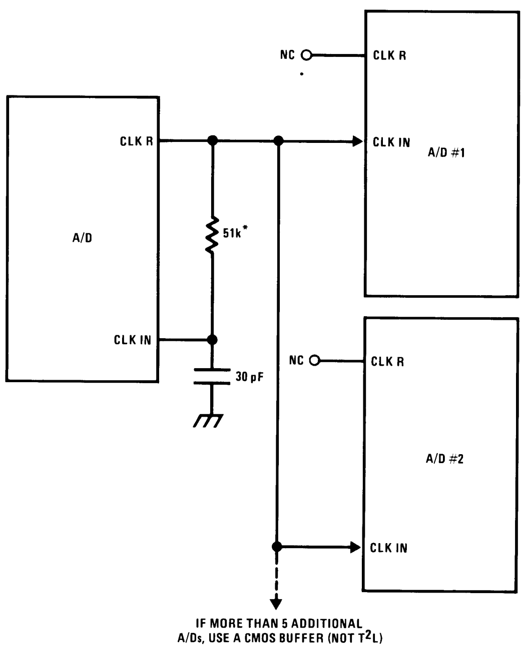
Typical Applications (Continued)

Digitizing a Current Flow



DS005671-62

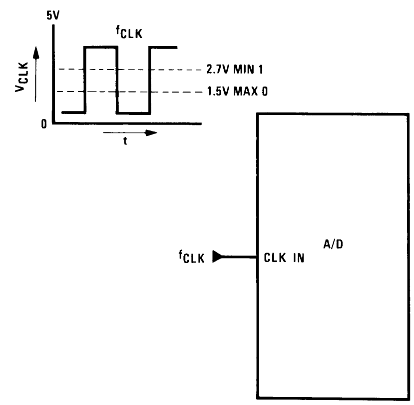
Self-Clocking Multiple A/Ds



DS005671-63

* Use a large R value
to reduce loading
at CLK R output.

External Clocking

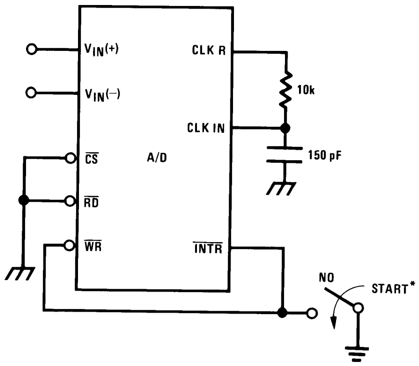


DS005671-64

100 kHz≤f_{CLK}≤1460 kHz

Typical Applications (Continued)

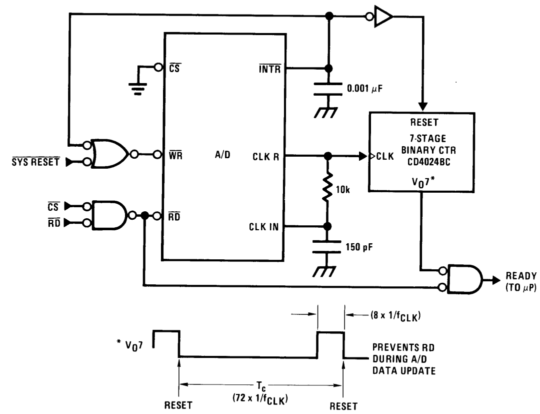
Self-Clocking in Free-Running Mode



DS005671-65

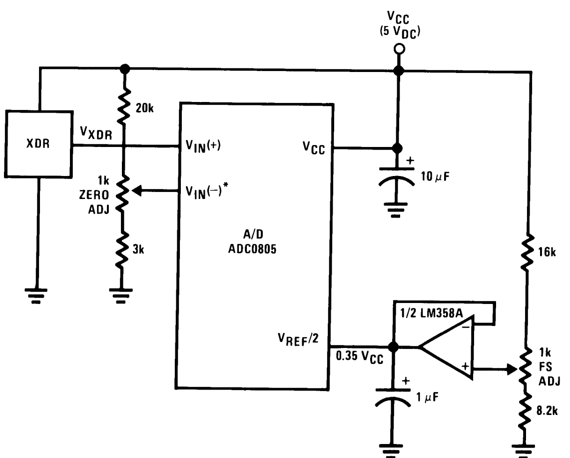
*After power-up, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation.

µP Interface for Free-Running A/D



DS005671-66

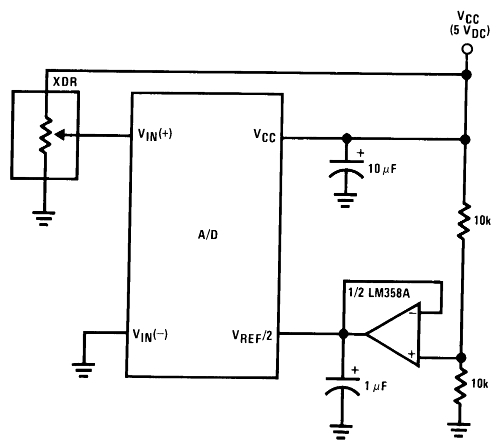
Operating with “Automotive” Ratiometric Transducers



DS005671-67

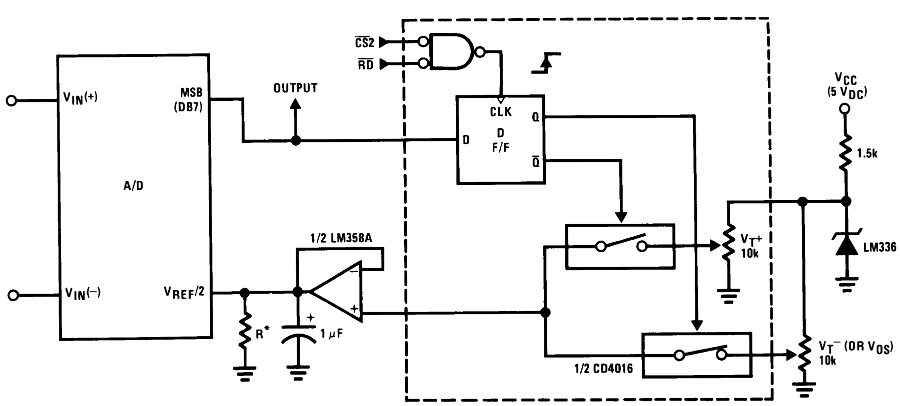
*$V_{IN}(-)$=0.15 V_{CC}
15% of $V_{CC} \leq V_{XDR} \leq$85% of V_{CC}

Ratiometric with V_{REF}/2 Forced



DS005671-68

µP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)

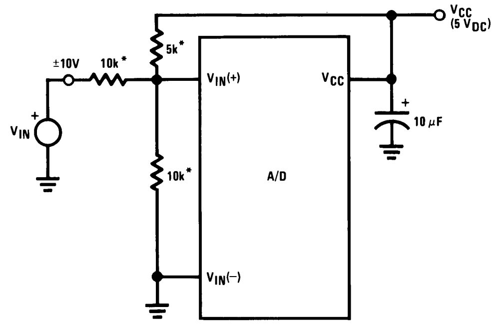


DS005671-69

*See *Figure 5* to select R value
DB7=“1” for $V_{IN}(+)>V_{IN}(-)+(V_{REF}/2)$
Omit circuitry within the dotted area if hysteresis is not needed

Typical Applications (Continued)

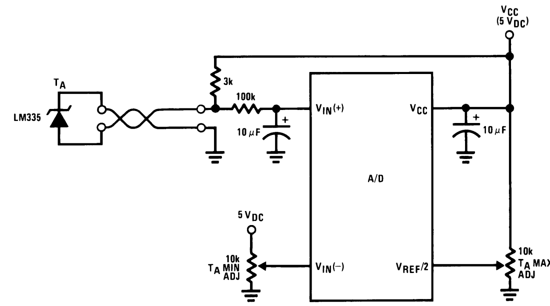
Handling ±10V Analog Inputs



DS005671-70

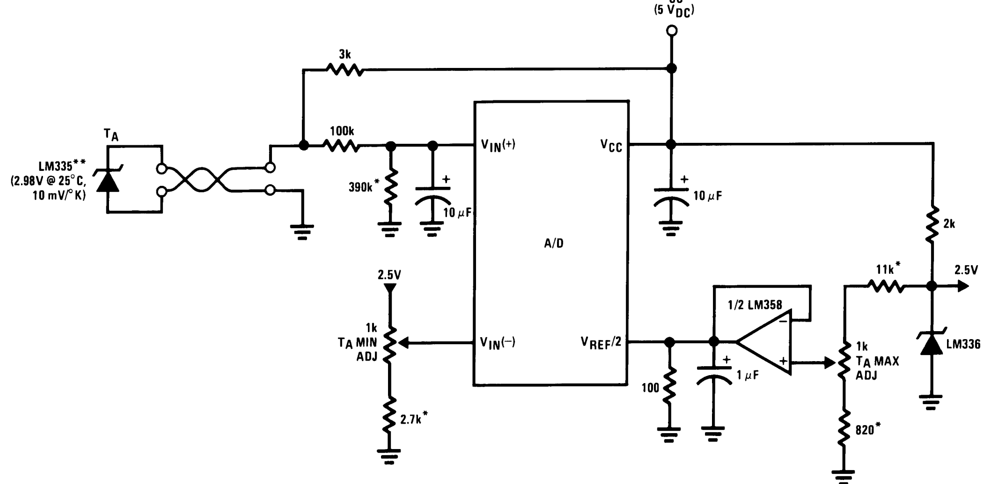
*Beckman Instruments #694-3-R10K resistor array

Low-Cost, µP Interfaced, Temperature-to-Digital Converter



DS005671-71

µP Interfaced Temperature-to-Digital Converter



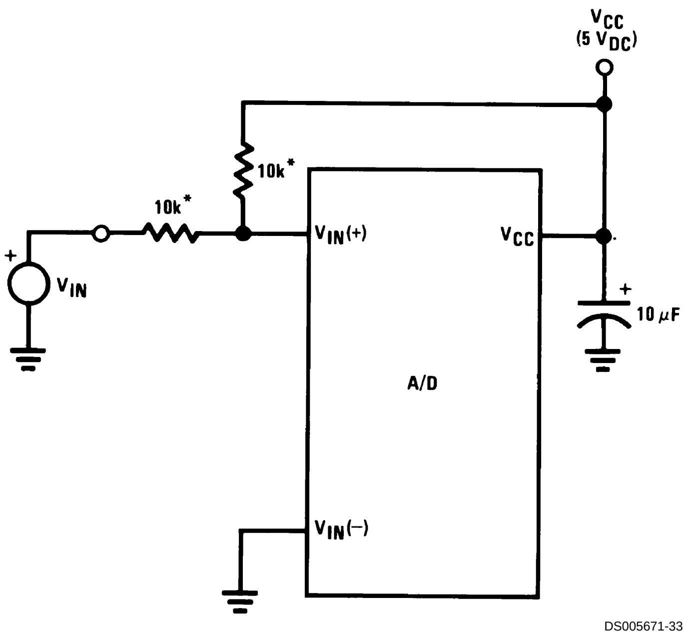
DS005671-72

*Circuit values shown are for 0˚C≤T_A≤+128˚C

***Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

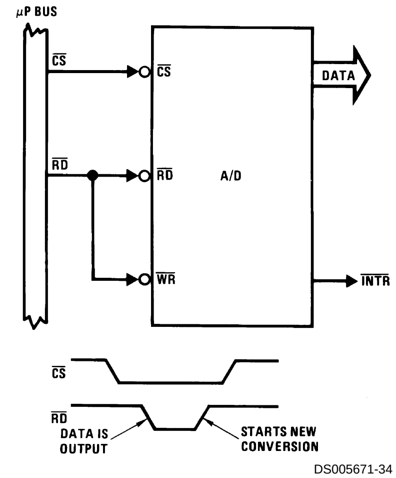
Typical Applications (Continued)

Handling ±5V Analog Inputs

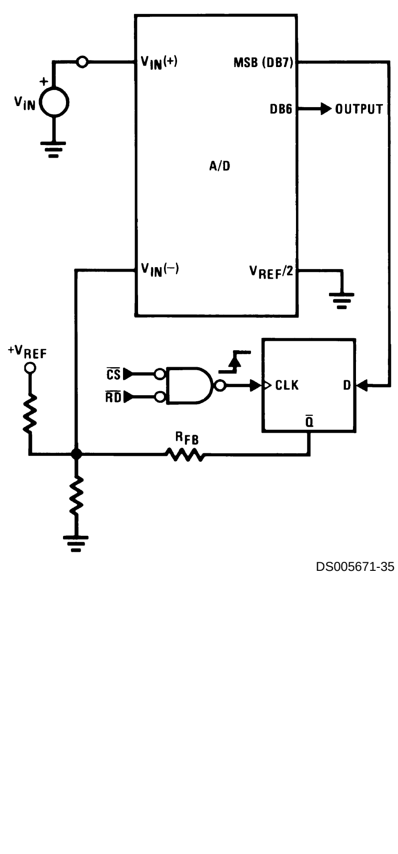


*Beckman Instruments #694-3-R10K resistor array

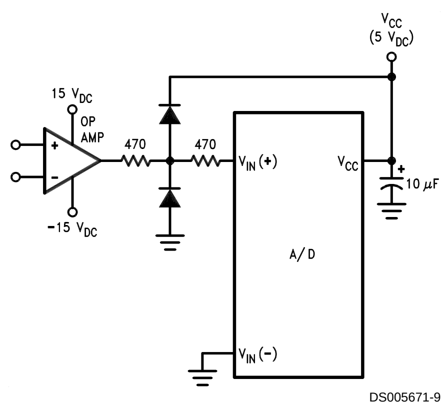
Read-Only Interface



μP Interfaced Comparator with Hysteresis



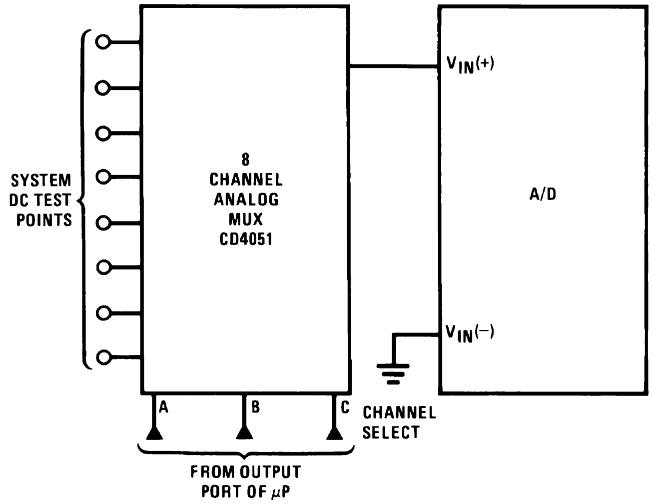
Protecting the Input



Diodes are 1N914

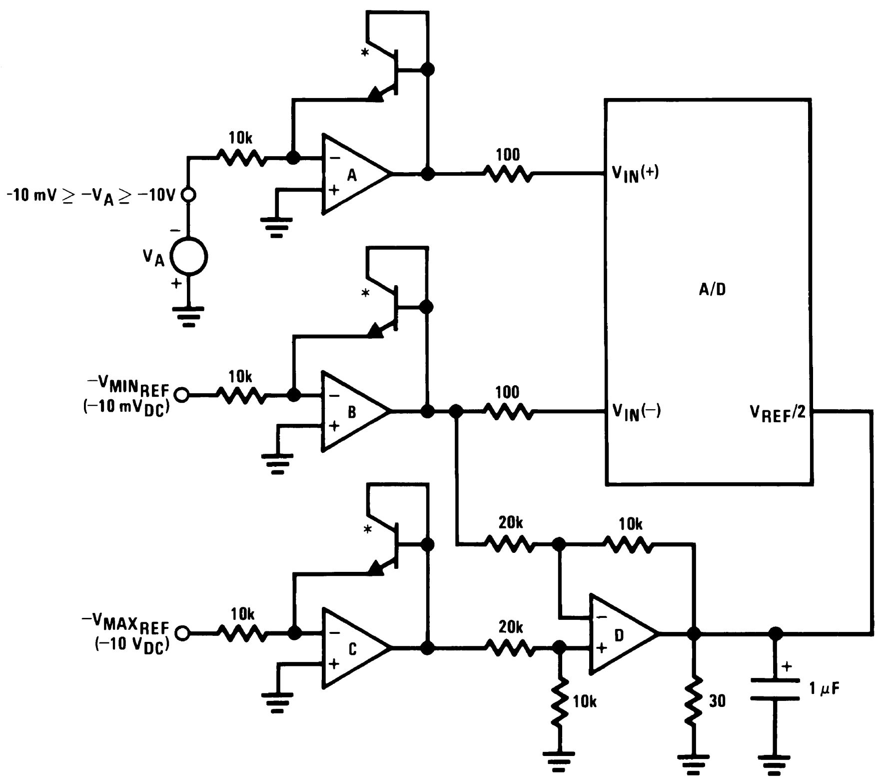
Typical Applications (Continued)

Analog Self-Test for a System



DS005671-36

A Low-Cost, 3-Decade Logarithmic Converter



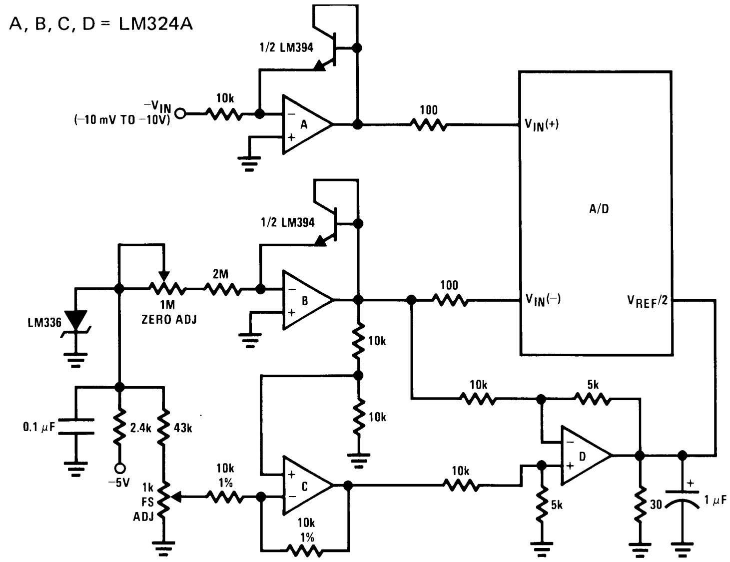
DS005671-37

*LM389 transistors

A, B, C, D = LM324A quad op amp

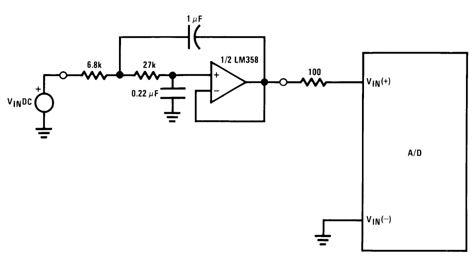
Typical Applications (Continued)

3-Decade Logarithmic A/D Converter



DS005671-73

Noise Filtering the Analog Input



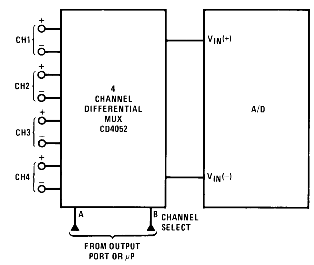
DS005671-74

f_C=20 Hz

Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter

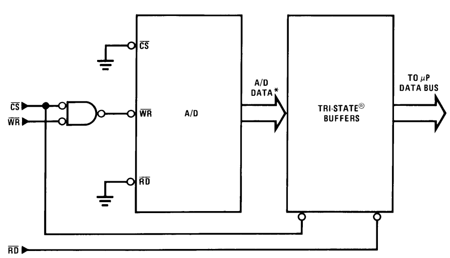
Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs



DS005671-75

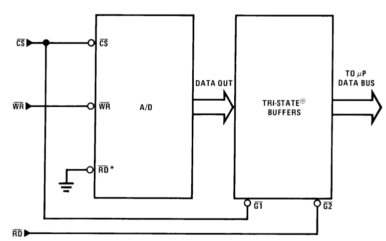
Output Buffers with A/D Data Enabled



DS005671-76

*A/D output data is updated 1 CLK period prior to assertion of $\overline{\text{INTR}}$

Increasing Bus Drive and/or Reducing Time on Bus

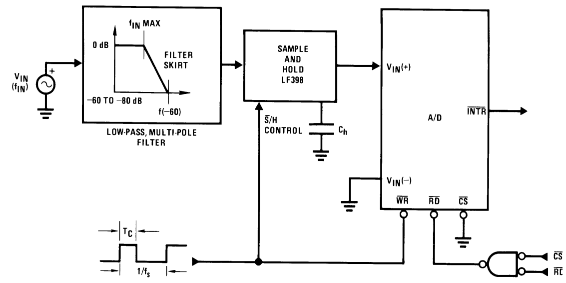


DS005671-77

*Allows output data to set-up at falling edge of $\overline{\text{CS}}$

Typical Applications (Continued)

Sampling an AC Input Signal

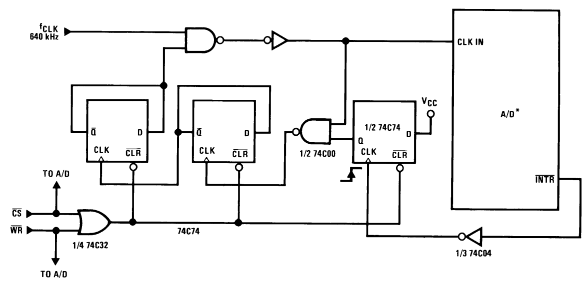


DS005671-78

Note 11: Oversample whenever possible [keep fs > 2f(−60)] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

Note 12: Consider the amplitude errors which are introduced within the passband of the filter.

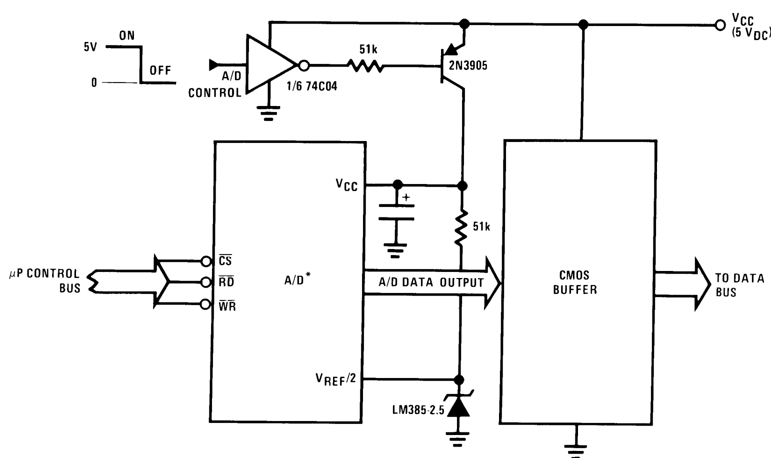
70% Power Savings by Clock Gating



DS005671-79

(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



DS005671-80

*Use ADC0801, 02, 03 or 05 for lowest power consumption.
Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.
Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, ...) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ±½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend

Functional Description (Continued)

±½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

Figure 2 shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 3* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1* is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.

Transfer Function **Error Plot**

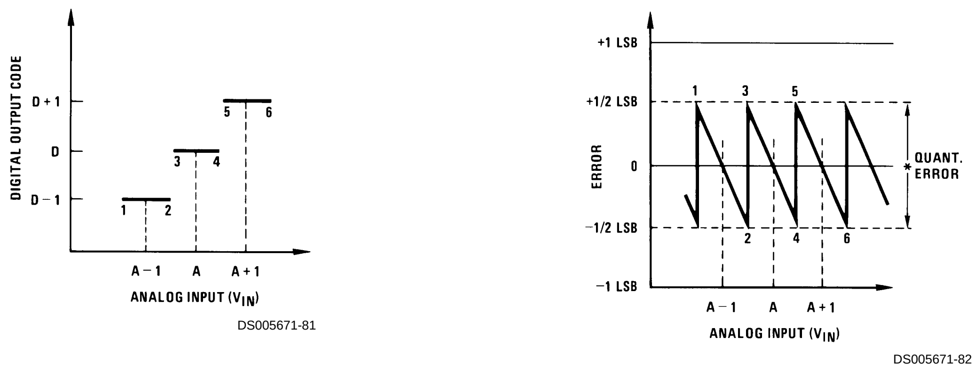


FIGURE 1. Clarifying the Error Specs of an A/D Converter Accuracy=±0 LSB: A Perfect A/D

Transfer Function **Error Plot**

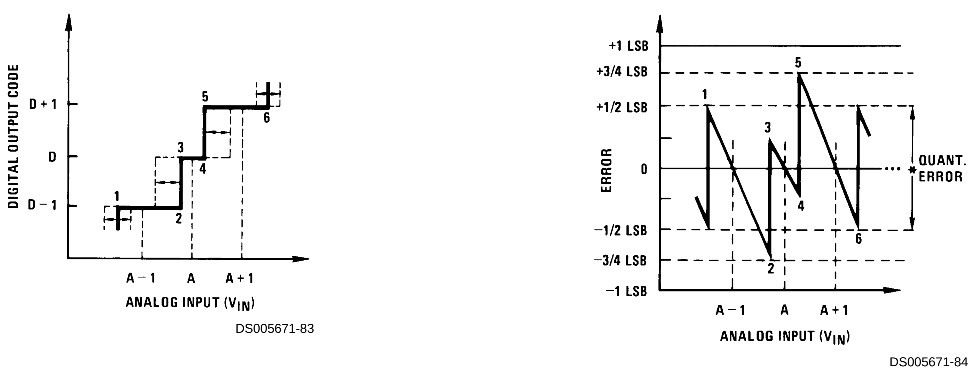
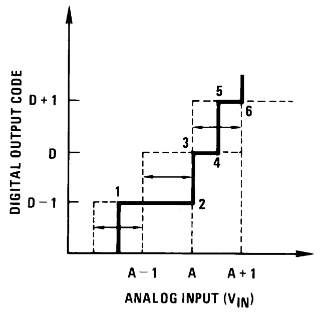


FIGURE 2. Clarifying the Error Specs of an A/D Converter Accuracy=±¼ LSB

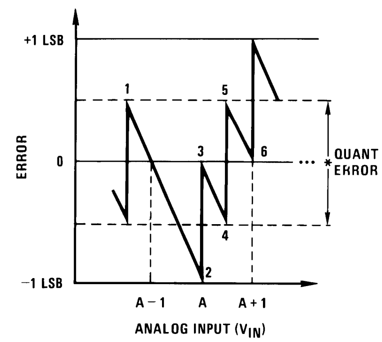
Functional Description (Continued)

Transfer Function



DS005671-85

Error Plot



DS005671-86

FIGURE 3. Clarifying the Error Specs of an A/D Converter Accuracy=±½ LSB

2.0 FUNCTIONAL DESCRIPTION

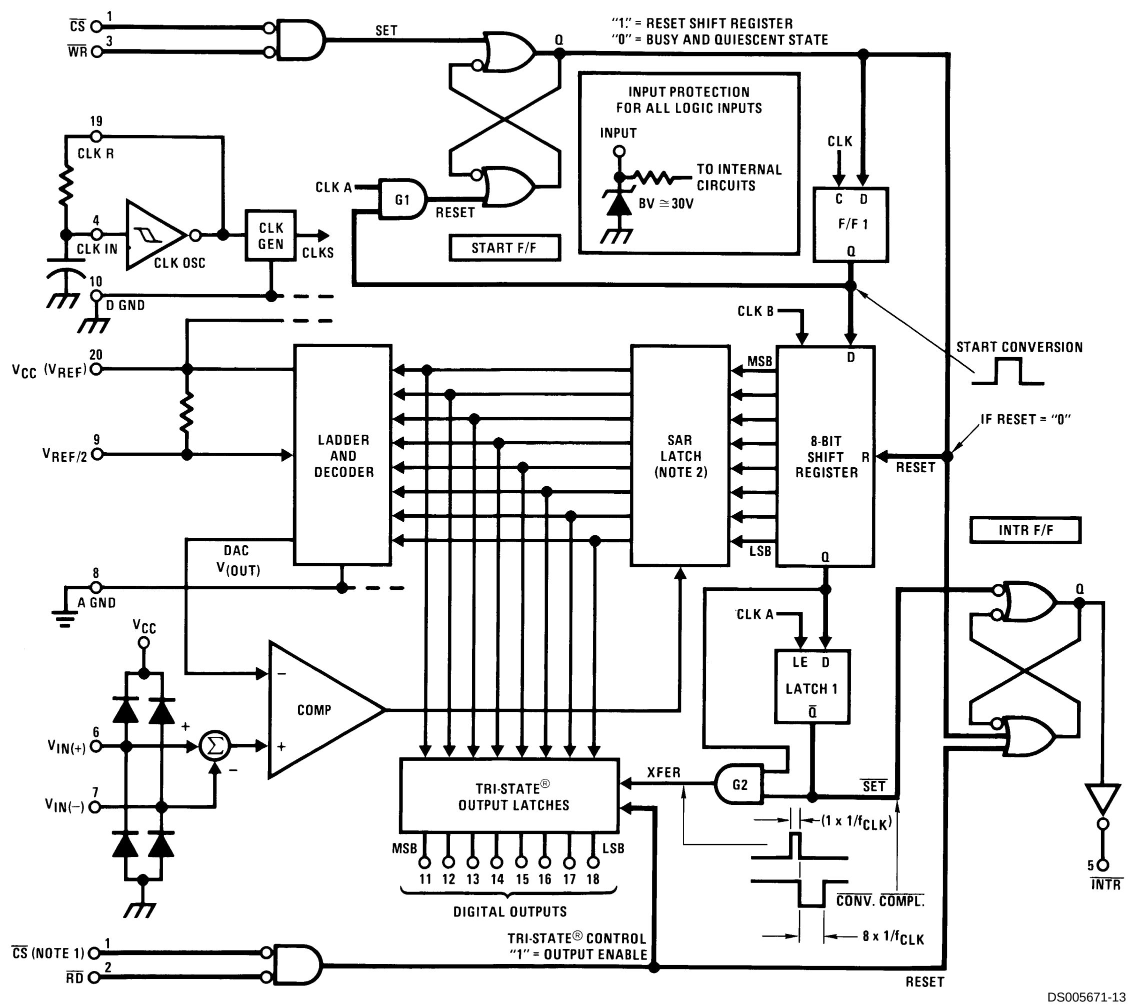
The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage [$V_{IN}(+) - V_{IN}(-)$] to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}$ =0. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition*.

A functional diagram of the A/D converter is shown in *Figure 4*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting “1” level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a “1” to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this “1” to the Q output of F/F1. The AND gate, G1, combines this “1” output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a “1”) the start F/F is reset and the 8-bit shift register then can have the “1” clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a “1” level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

Functional Description (Continued)



Note 13: $\overline{CS}$ shown twice for clarity.

Note 14: SAR = Successive Approximation Register.

FIGURE 4. Block Diagram

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at ⅛ of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard T^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

Functional Description (Continued)

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)\,(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right)$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}\,(f_{CLK})]}{(2\pi f_{cm})\,(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})\,(640 \times 10^3)}{(6.28)\,(60)\,(4.5)}$$

which gives

$V_P \simeq 1.9V$.

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

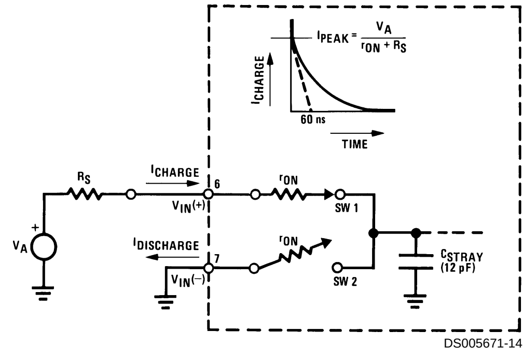
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3 1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 5*.



r_{ON} of SW 1 and SW 2 ≃ 5 kΩ

$r = r_{ON}\,C_{STRAY}$ ≃ 5 kΩ x 12 pF = 60 ns

FIGURE 5. Analog Input Impedance

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of V_{CC}+50 mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 µA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (≤ 1 kΩ), a 0.1 µF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long

Functional Description (Continued)

wire. A 100Ω series resistor can be used to isolate this capacitor — both the R and C are placed outside the feedback loop — from the output of an op amp, if used.

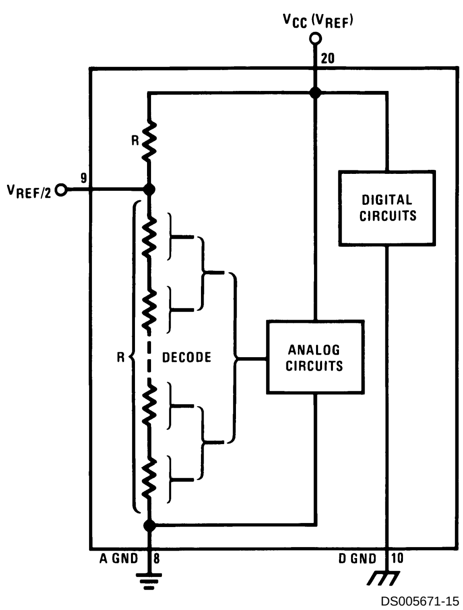
2.3.4 Noise

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading — see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 6*.



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FIGURE 6. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

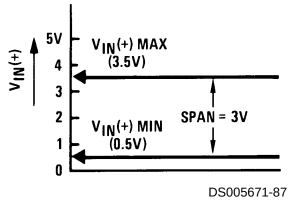
An example of the use of an adjusted reference voltage is to accommodate a reduced span — or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 7*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

2.4.2 Reference Accuracy Requirements

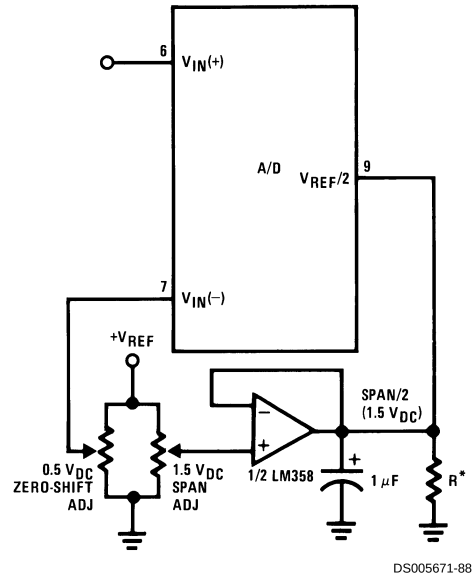
The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of ±10 mV_{DC} will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over 0˚C≤T_A≤+70˚C. Other temperature range parts are also available.

Functional Description (Continued)



a) Analog Input Signal Example



*Add if $V_{REF}/2 \leq 1$ V_{DC} with LM358 to draw 3 mA to ground.

b) Accommodating an Analog Input from 0.5V (Digital Out = 00_{HEX}) to 3.5V (Digital Out=FF_{HEX})

FIGURE 7. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2$=2.500 V_{DC}).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB=analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\text{ fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX}=The high end of the analog input range

and

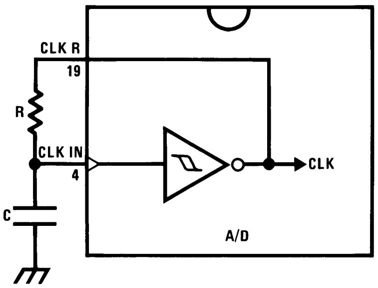
V_{MIN}=the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 8*.

Functional Description (Continued)



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$$f_{CLK} \cong \frac{1}{1.1\ RC}$$

$$R \cong 10\ k\Omega$$

FIGURE 8. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output simply remains at the “1” level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 µF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

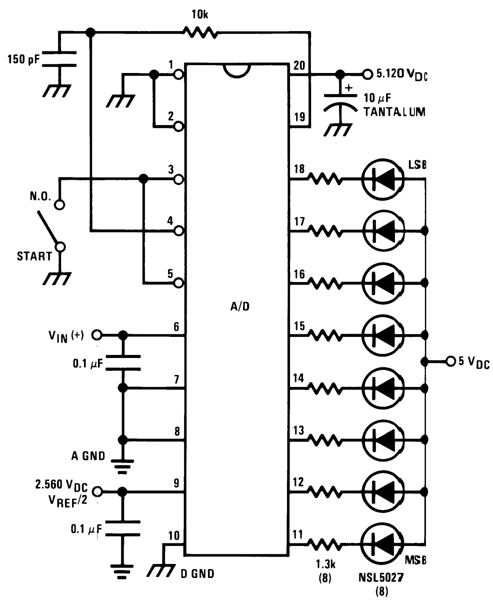
There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 9*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120–1½ LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). *Table 1* shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the “VMS” and “VLS” columns in *Table 1*, the nominal value of the digital display (when $V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

Functional Description (Continued)



DS005671-18

FIGURE 9. Basic A/D Tester

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A–C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 11*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

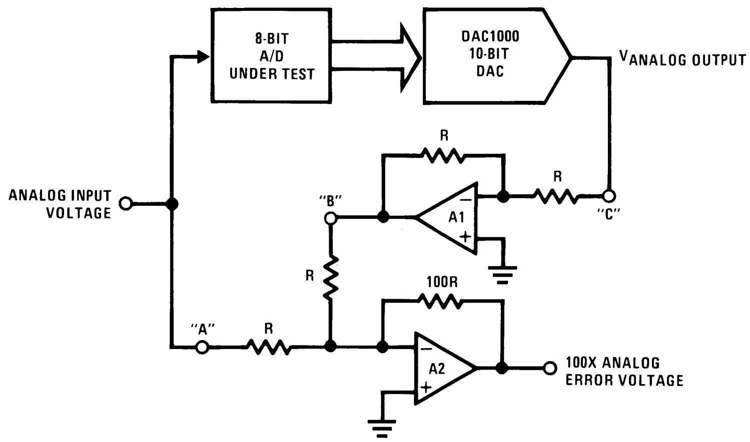
4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

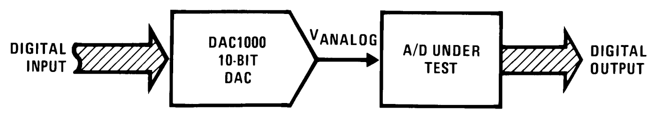
This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 12*.

Functional Description (Continued)



DS005671-89

FIGURE 10. A/D Tester with Analog Error Output



DS005671-90

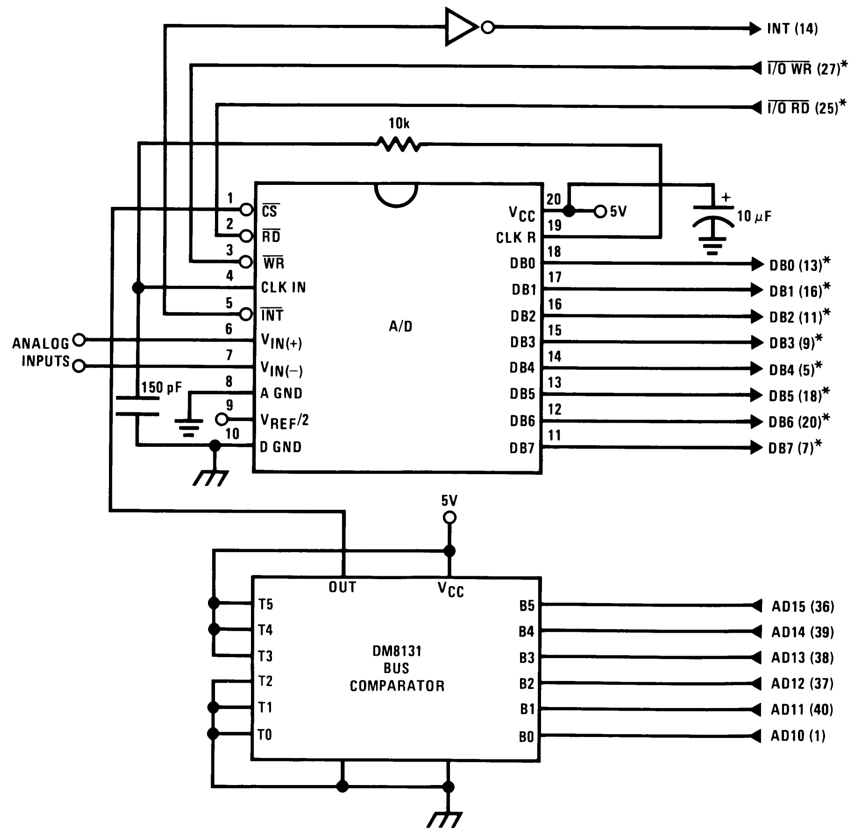
FIGURE 11. Basic "Digital" A/D Tester

TABLE 1. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY				FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2=2.560\ V_{DC}$	
					MS GROUP	LS GROUP	VMS GROUP (Note 15)	VLS GROUP (Note 15)
F	1	1	1	1	15/16	15/256	4.800	0.300
E	1	1	1	0	7/8	7/128	4.480	0.280
D	1	1	0	1	13/16	13/256	4.160	0.260
C	1	1	0	0	3/4	3/64	3.840	0.240
B	1	0	1	1	11/16	11/256	3.520	0.220
A	1	0	1	0	5/8	5/128	3.200	0.200
9	1	0	0	1	9/16	9/256	2.880	0.180
8	1	0	0	0	1/2	1/32	2.560	0.160
7	0	1	1	1	7/16	7/256	2.240	0.140
6	0	1	1	0	3/8	3/128	1.920	0.120
5	0	1	0	1	5/16	2/256	1.600	0.100
4	0	1	0	0	1/4	1/64	1.280	0.080
3	0	0	1	1	3/16	3/256	0.960	0.060
2	0	0	1	0	1/8	1/128	0.640	0.040
1	0	0	0	1	1/16	1/256	0.320	0.020
0	0	0	0	0			0	0

Note 15: Display Output=VMS Group + VLS Group

Functional Description (Continued)



Note 16: *Pin numbers for the DP8228 system controller, others are INS8080A.

Note 17: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 12. ADC0801_INS8080A CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 12* ADC0801–INS8080A CPU INTERFACE

```
0038    C3 00 03   RST 7:               JMP   LD DATA
  •        •         •
  •        •         •
0100    21 00 02   START:               LXI H 0200H      ; HL pair will point to
                                                         ; data storage locations
0103    31 00 04   RETURN:              LXI SP 0400H     ; Initialize stack pointer (Note 1)
0106    7D                              MOV A, L         ; Test # of bytes entered
0107    FE 0F                           CPI 0F H         ; If # = 16. JMP to
0109    CA 13 01                        JZ CONT          ; user program
010C    D3 E0                           OUT E0 H         ; Start A/D
010E    FB                              EI               ; Enable interrupt
010F    00         LOOP:                NOP              ; Loop until end of
0110    C3 0F 01                        JMP LOOP         ; conversion
0113       •       CONT:                  •
  •        •         •                    •
  •        •       (User program to       •
  •        •       process data)          •
  •        •         •                    •
  •        •         •                    •
0300    DB E0      LD DATA:             IN E0 H          ; Load data into accumulator
0302    77                              MOV M, A         ; Store data
0303    23                              INX H            ; Increment storage pointer
0304    C3 03 01                        JMP RETURN
```

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Note 18: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 19: All address used were arbitrarily chosen.

The standard control bus signals of the 8080 $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 12* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs — one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 13*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{RD}$, $\overline{WR}$ and $\overline{INT}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

Functional Description (Continued)

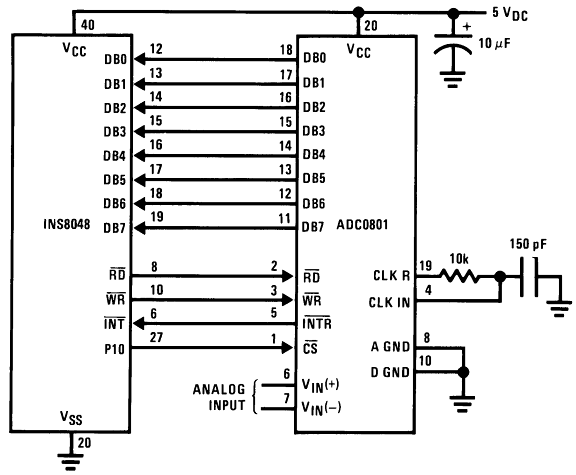


FIGURE 13. INS8048 Interface

SAMPLE PROGRAM FOR *Figure 13* **INS8048 INTERFACE**

```
04 10                JMP     10H         : Program starts at addr 10
                     ORG     3H
04 50                JMP     50H         ; Interrupt jump vector
                     ORG     10H         ; Main program
99 FE                ANL     P1, #0FEH   ; Chip select
81                   MOVX    A, @R1      ; Read in the 1st data
                                         ; to reset the intr
89 01     START:     ORL     P1, #1      ; Set port pin high
B8 20                MOV     R0, #20H    ; Data address
B9 FF                MOV     R1, #0FFH   ; Dummy address
BA 10                MOV     R2, #10H    ; Counter for 16 bytes
23 FF     AGAIN:     MOV     A, #0FFH    ; Set ACC for intr loop
99 FE                ANL     P1, #0FEH   ; Send CS (bit 0 of P1)
91                   MOVX    @R1, A      ; Send WR out
05                   EN      I           ; Enable interrupt
96 21     LOOP:      JNZ     LOOP        ; Wait for interrupt
EA 1B                DJNZ    R2, AGAIN   ; If 16 bytes are read
00                   NOP                 ; go to user's program
00                   NOP
                     ORG     50H
81        INDATA:    MOVX    A, @R1      ; Input data, CS still low
A0                   MOV     @R0, A      ; Store in memory
18                   INC     R0          ; Increment storage counter
89 01                ORL     P1, #1      ; Reset CS signal
27                   CLR     A           ; Clear ACC to get out of
93                   RETR                ; the interrupt loop
```

DS005671-A0

4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 14*.

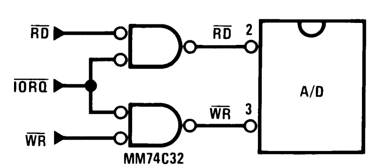


FIGURE 14. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to

Functional Description (Continued)

A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived fom the ϕ2 clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 15* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 16* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

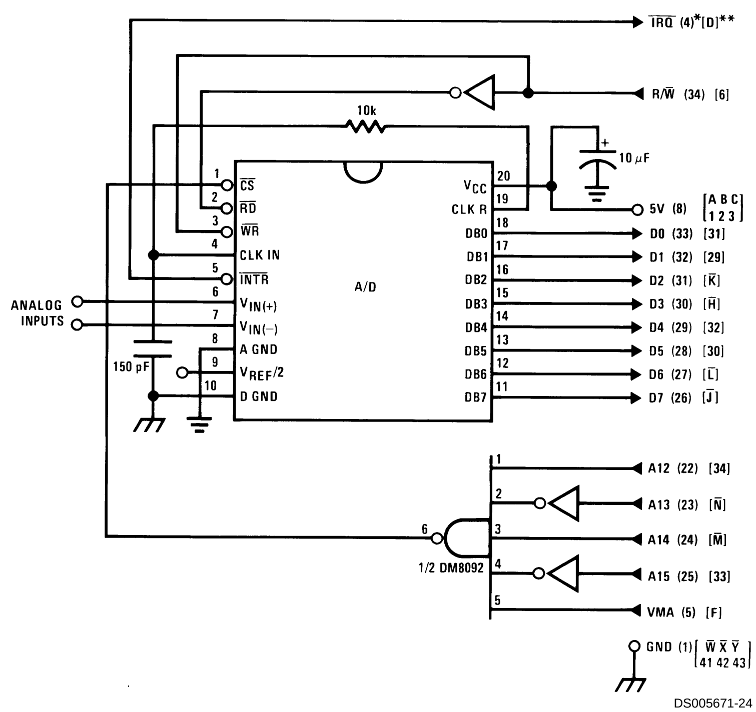
A sample interface program equivalent to the previous one is shown below *Figure 16*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 17*.



Note 20: Numbers in parentheses refer to MC6800 CPU pin out.

Note 21: Number or letters in brackets refer to standard M6800 system common bus code.

FIGURE 15. ADC0801-MC6800 CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 15* ADC0801-MC6800 CPU INTERFACE

```
0010   DF 36      DATAIN   STX    TEMP2     ; Save contents of X
0012   CE 00 2C            LDX    #$002C    ; Upon IRQ low CPU
0015   FF FF F8            STX    $FFF8     ; jumps to 002C
0018   B7 50 00            STAA   $5000     ; Start ADC0801
001B   0E                  CLI
001C   3E         CONVRT   WAI              ; Wait for interrupt
001D   DE 34               LDX    TEMP1
001F   8C 02 0F            CPX    #$020F    ; Is final data stored?
0022   27 14               BEQ    ENDP
0024   B7 50 00            STAA   $5000     ; Restarts ADC0801
0027   08                  INX
0028   DF 34               STX    TEMP1
002A   20 F0               BRA    CONVRT
002C   DE 34      INTRPT   LDX    TEMP1
002E   B6 50 00            LDAA   $5000     ; Read data
0031   A7 00               STAA   X         ; Store it at X
0033   3B                  RTI
0034   02 00      TEMP1    FDB    $0200     ; Starting address for
                                            ; data storage
0036   00 00      TEMP2    FDB    $0000
0038   CE 02 00   ENDP     LDX    #$0200    ; Reinitialize TEMP1
003B   DF 34               STX    TEMP1
003D   DE 36               LDX    TEMP2
003F   39                  RTS              ; Return from subroutine
                                            ; To user's program
```

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Note 22: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

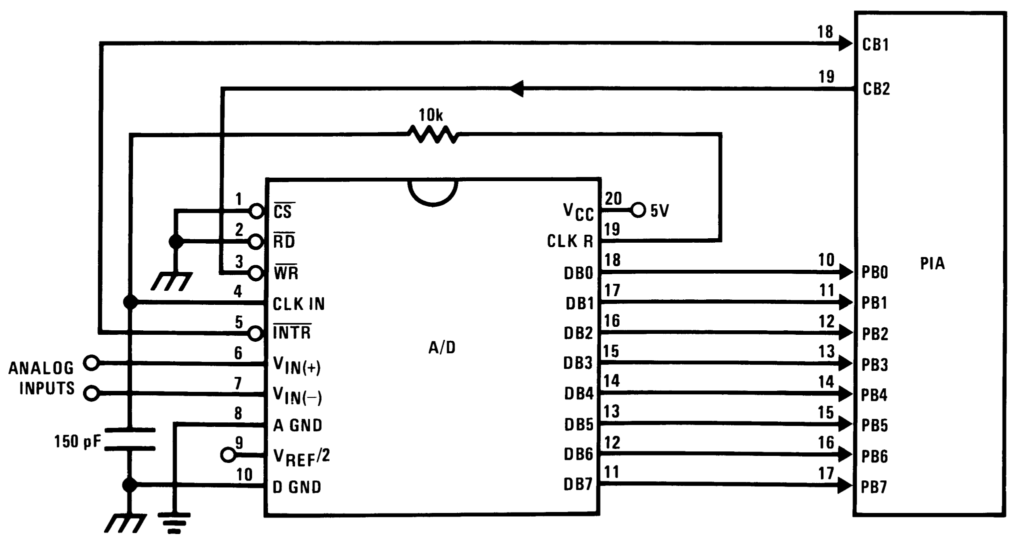


FIGURE 16. ADC0801–MC6820 PIA Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR ***Figure 16*** **ADC0801–MC6820 PIA INTERFACE**

```
0010   CE 00 38   DATAIN   LDX    #$0038    ; Upon IRQ low CPU
0013   FF FF F8            STX    $FFF8     ; jumps to 0038
0016   B6 80 06            LDAA   PIAORB    ; Clear possible IRQ flags
0019   4F                  CLRA
001A   B7 80 07            STAA   PIACRB
001D   B7 80 06            STAA   PIAORB    ; Set Port B as input
0020   0E                  CLI
0021   C6 34               LDAB   #$34
0023   86 3D               LDAA   #$3D
0025   F7 80 07   CONVRT   STAB   PIACRB    ; Starts ADC0801
0028   B7 80 07            STAA   PIACRB
002B   3E                  WAI              ; Wait for interrupt
002C   DE 40               LDX    TEMP1
002E   8C 02 0F            CPX    #$020F    ; Is final data stored?
0031   27 0F               BEQ    ENDP
0033   08                  INX
0034   DF 40               STX    TEMP1
0036   20 ED               BRA    CONVRT
0038   DE 40      INTRPT   LDX    TEMP1
003A   B6 80 06            LDAA   PIAORB    ; Read data in
003D   A7 00               STAA   X         ; Store it at X
003F   3B                  RTI
0040   02 00      TEMP1    FDB    $0200     ; Starting address for
                                            ; data storage
0042   CE 02 00   ENDP     LDX    #$0200    ; Reinitialize TEMP1
0045   DF 40               STX    TEMP1
0047   39                  RTS              ; Return from subroutine
                  PIAORB   EQU    $8006     ; To user's program
                  PIACRB   EQU    $8007
```

DS005671-A2

The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

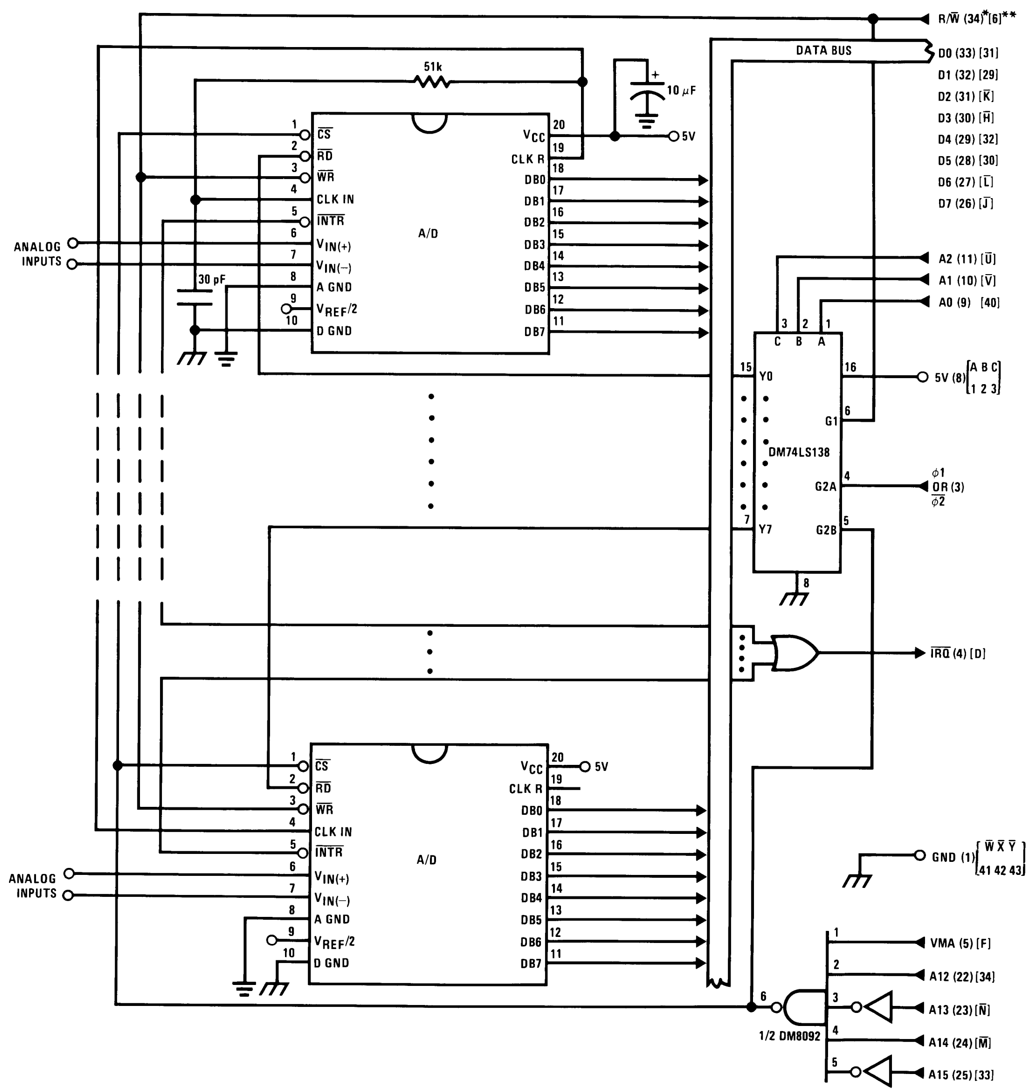
All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{\text{CS}}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

Functional Description (Continued)



Note 23: Numbers in parentheses refer to MC6800 CPU pin out.

Note 24: Numbers of letters in brackets refer to standard M6800 system common bus code.

FIGURE 17. Interfacing Multiple A/Ds in an MC6800 System

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 17* INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0010	DF 44	DATAIN	STX	TEMP	; Save Contents of X
0012	CE 00 2A		LDX	#$002A	; Upon $\overline{\text{IRQ}}$ LOW CPU
0015	FF FF F8		STX	$FFF8	; Jumps to 002A
0018	B7 50 00		STAA	$5000	; Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		; Wait for interrupt
001D	CE 50 00		LDX	#$5000	
0020	DF 40		STX	INDEX1	; Reset both INDEX
0022	CE 02 00		LDX	#$0200	; 1 and 2 to starting
0025	DF 42		STX	INDEX2	; addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		; Return from subroutine
002A	DE 40	INTRPT	LDX	INDEX1	; INDEX1 → X
002C	A6 00		LDAA	X	; Read data in from A/D at X
002E	08		INX		; Increment X by one
002F	DF 40		STX	INDEX1	; X → INDEX1
0031	DE 42		LDX	INDEX2	; INDEX2 → X

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SAMPLE PROGRAM FOR *Figure 17* INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0033	A7 00		STAA	X	; Store data at X
0035	8C 02 07		CPX	#$0207	; Have all A/D's been read?
0038	27 05		BEQ	RETURN	; Yes: branch to RETURN
003A	08		INX		; No: increment X by one
003B	DF 42		STX	INDEX2	; X → INDEX2
003D	20 EB		BRA	INTRPT	; Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	$5000	; Starting address for A/D
0042	02 00	INDEX2	FDB	$0200	; Starting address for data storage
0044	00 00	TEMP	FDB	$0000	

DS005671-A4

Note 25: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 18* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 µV for ¼ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} +$$

$$\underbrace{(V_{OS_2} - V_{OS_1} - V_{OS_3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

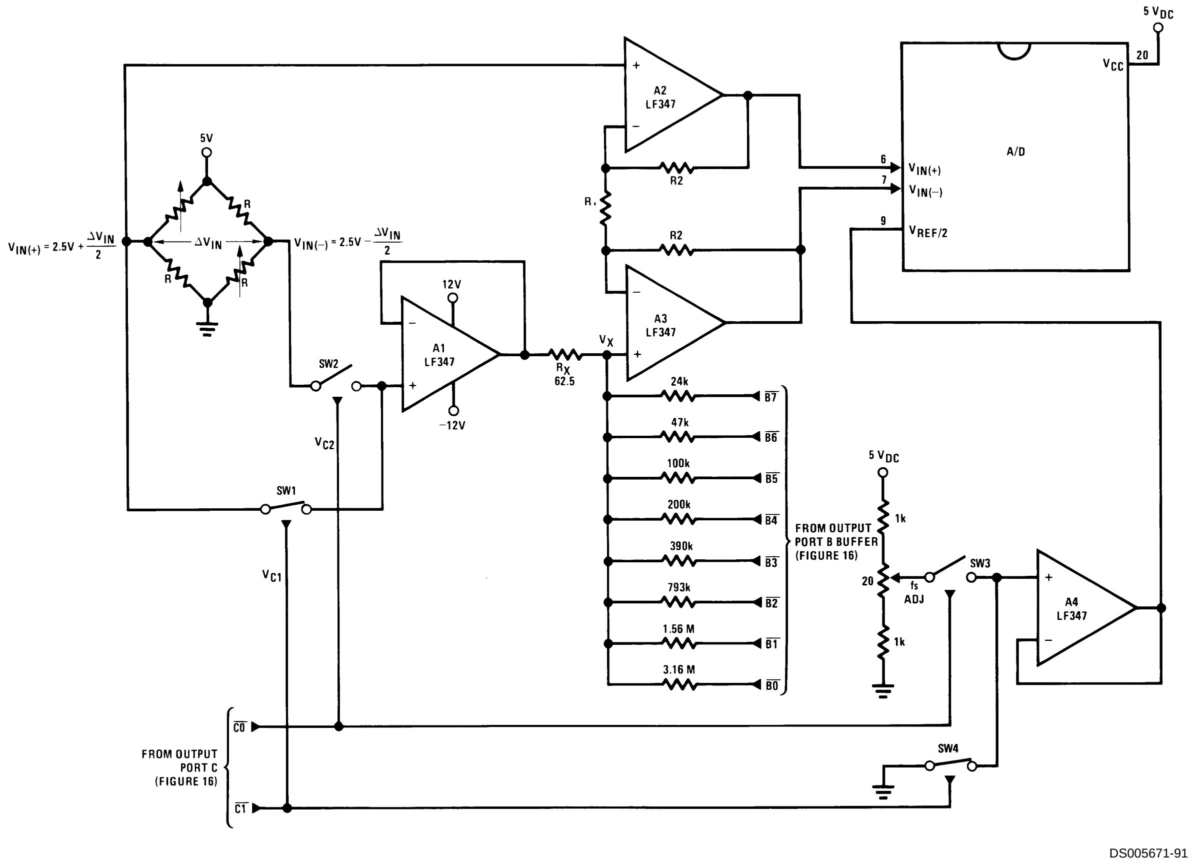
where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 19*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_x increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on

Functional Description (Continued)

any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ±12 mV with a resolution of 50 µV, which will null the offset error term to ¼ LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.



Note 26: R2 = 49.5 R1

Note 27: Switches are LMC13334 CMOS analog switches.

Note 28: The 9 resistors used in the auto-zero section can be ±5% tolerance.

FIGURE 18. Gain of 100 Differential Transducer Preamp

Functional Description (Continued)

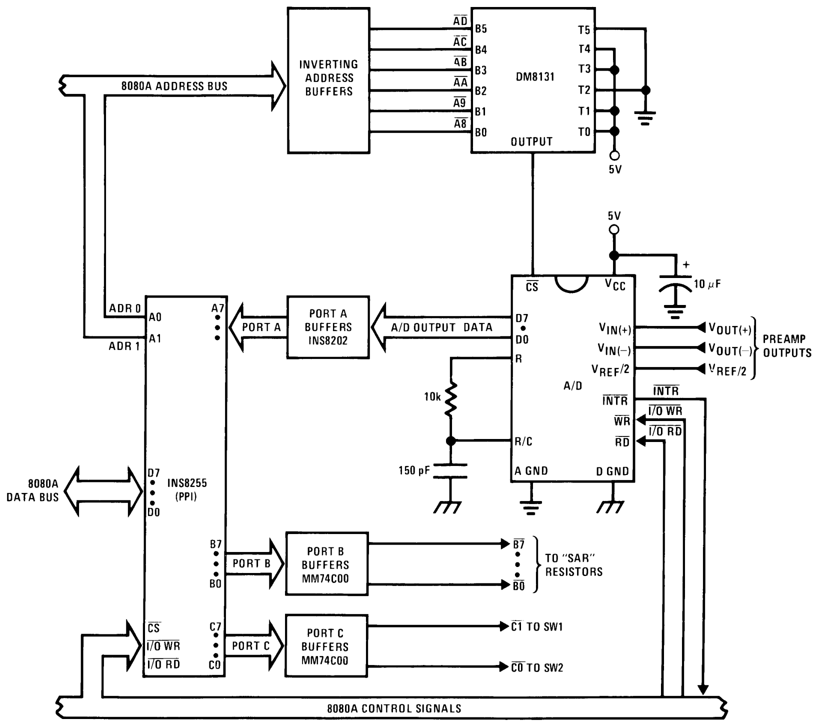


FIGURE 19. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 20*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input $[V_{IN}(-) \geq V_{IN}(+)]$. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 21.* All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 22* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

Functional Description (Continued)

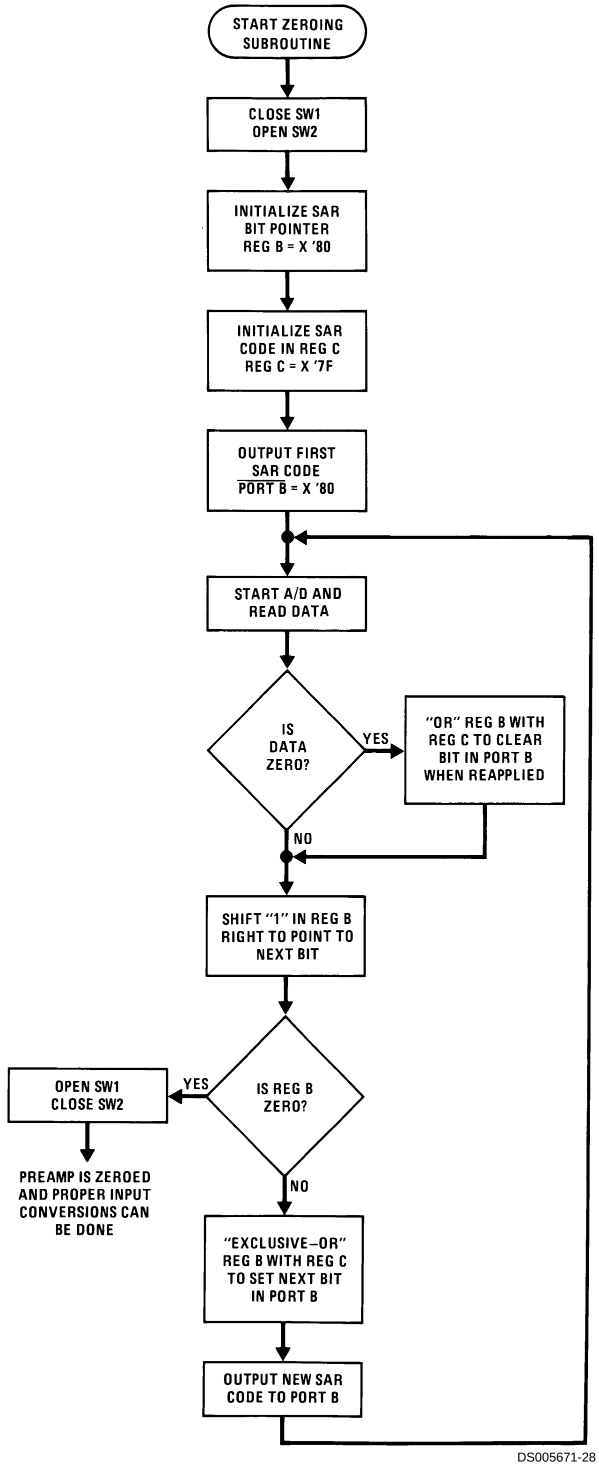


FIGURE 20. Flow Chart for Auto-Zero Routine

Functional Description (Continued)

```
3D00  3E90     MVI 90
3D02  D3E7     Out Control Port                            ; Program PPI
3D04  2601     MVI H 01           Auto-Zero Subroutine
3D06  7C       MOV A,H
3D07  D3E6     OUT C                                       ; Close SW1 open SW2
3D09  0680     MVI B 80                                    ; Initialize SAR bit pointer
3D0B  3E7F     MVI A 7F                                    ; Initialize SAR code
3D0D  4F       MOV C,A            Return
3D0E  D3E5     OUT B                                       ; Port B = SAR code
3D10  31AA3D   LXI SP 3DAA        Start                    ; Dimension stack pointer
3D13  D3E4     OUT A                                       ; Start A/D
3D15  FB       IE
3D16  00       NOP                Loop                     ; Loop until INT asserted
3D17  C3163D   JMP Loop
3D1A  7A       MOV A,D            Auto-Zero
3D1B  C600     ADI 00
3D1D  CA2D3D   JZ Set C                                    ; Test A/D output data for zero
3D20  78       MOV A,B            Shift B
3D21  F600     ORI 00                                      ; Clear carry
3D23  1F       RAR                                         ; Shift "1" in B right one place
3D24  FE00     CPI 00                                      ; Is B zero? If yes last
3D26  CA373D   JZ Done                                     ; approximation has been made
3D29  47       MOV B,A
3D2A  C3333D   JMP New C
3D2D  79       MOV A,C            Set C
3D2E  B0       ORA B                                       ; Set bit in C that is in same
3D2F  4F       MOV C,A                                     ; position as "1" in B
3D30  C3203D   JMP Shift B
3D33  A9       XRA C              New C                    ; Clear bit in C that is in
3D34  C30D3D   JMP Return                                  ; same position as "1" in B
3D37  47       MOV B,A            Done                     ; then output new SAR code.
3D38  7C       MOV A,H                                     ; Open SW1, close SW2 then
3D39  EE03     XRI 03                                      ; proceed with program. Preamp
3D3B  D3E6     OUT C                                       ; is now zeroed.
3D3D           •                  Normal
               •
               •
               Program for processing
               proper data values
3C3D  DBE4     IN A               Read A/D Subroutine      ; Read A/D data
3C3F  EEFF     XRI FF                                      ; Invert data
3C41  57       MOV D,A
3C42  78       MOV A,B                                     ; Is B Reg = 0? If not stay
3C43  E6FF     ANI FF                                      ; in auto zero subroutine
3C45  C21A3D   JNZ Auto-Zero
3C48  C33D3D   JMP Normal
```

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Note 29: All numerical values are hexadecimal representations.

FIGURE 21. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode (Continued)

The following notes apply:

- It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.
- The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.
- A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.
- The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.
- The peripherals of concern are mapped into I/O space with the following port assignments:

Functional Description (Continued)

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

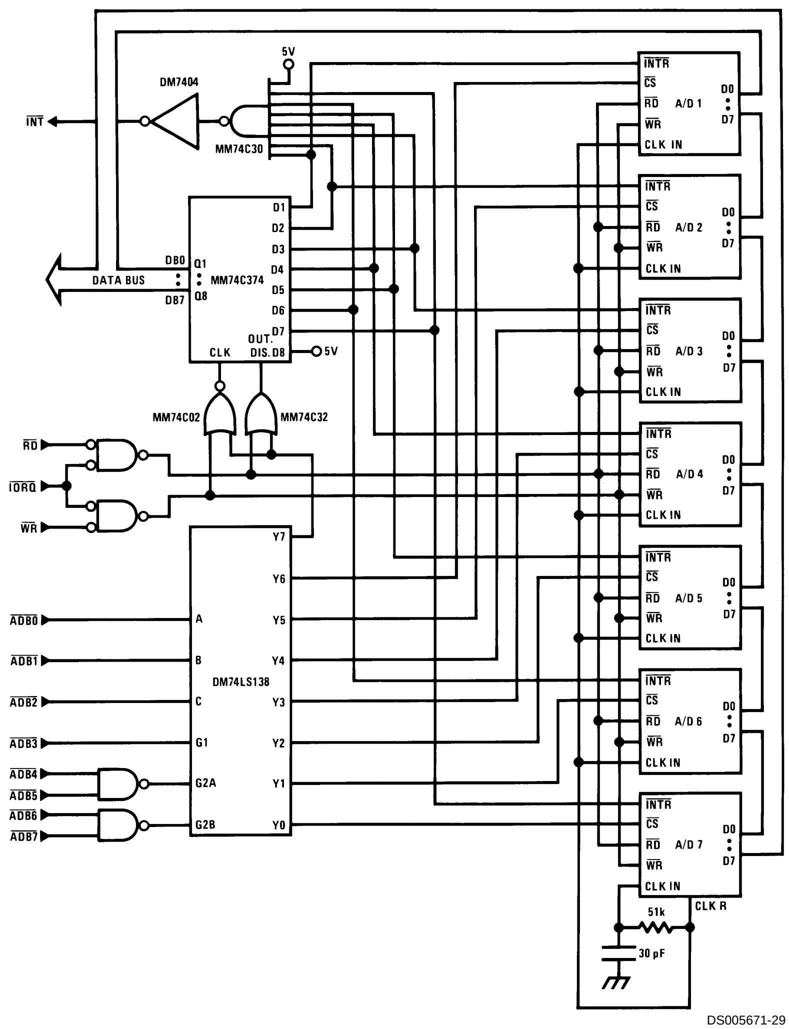


FIGURE 22. Multiple A/Ds with Z-80 Type Microprocessor

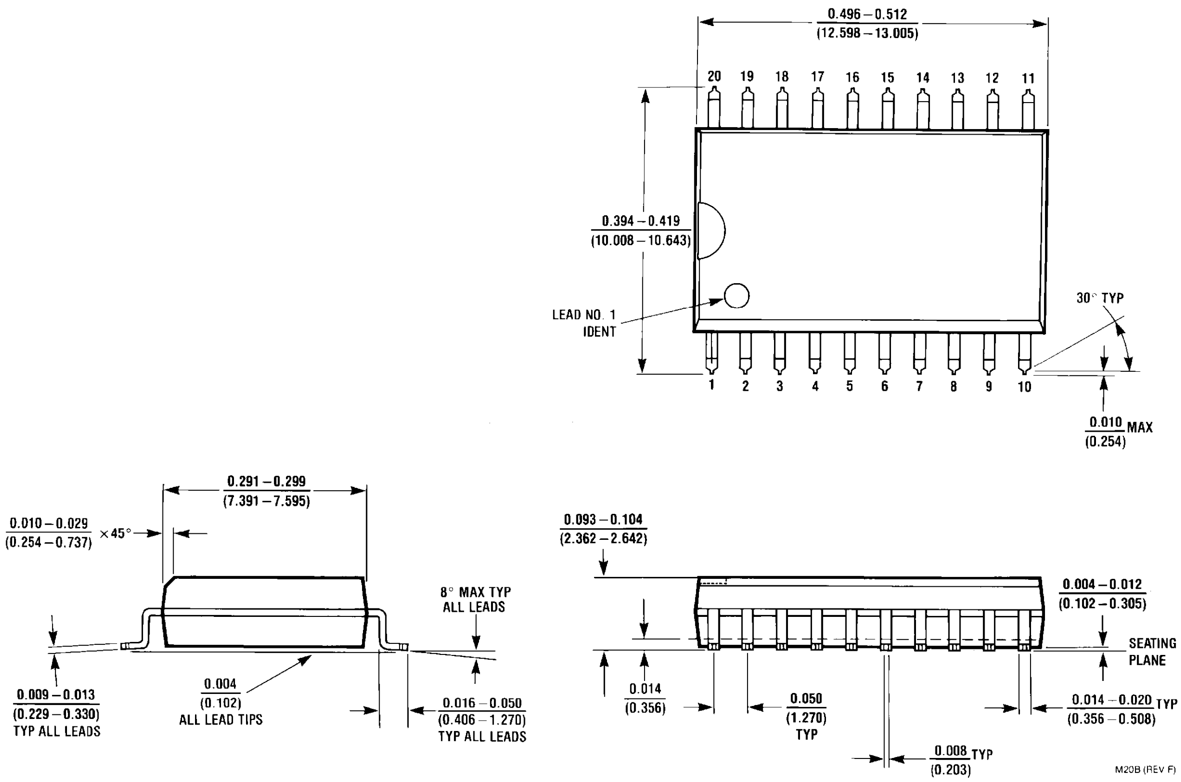
Functional Description (Continued)

INTERRUPT SERVICING SUBROUTINE

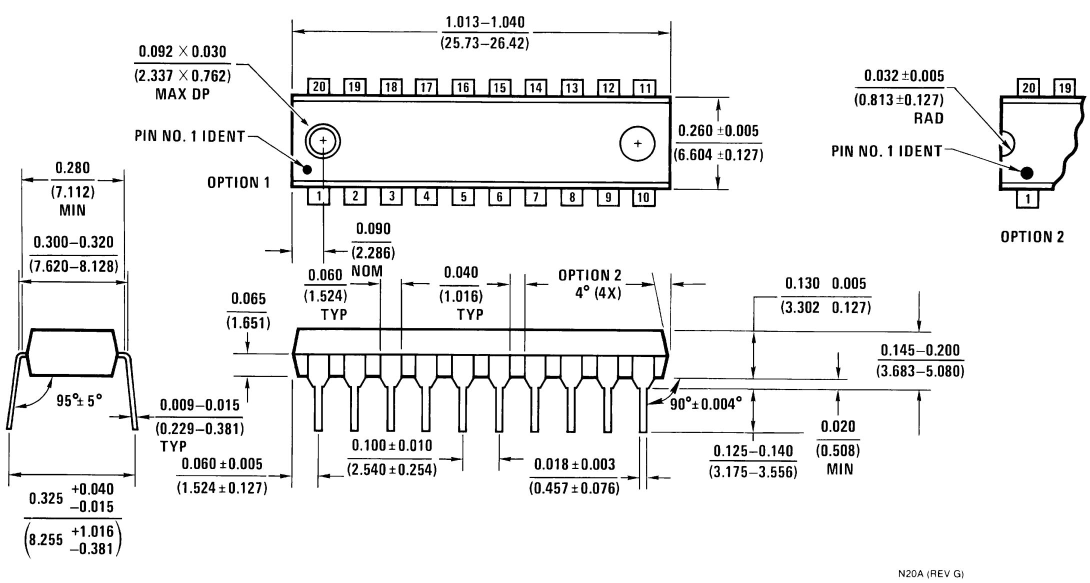
```
LOC   OBJ CODE            SOURCE          COMMENT
                          STATEMENT
0038  E5                  PUSH HL         ; Save contents of all registers affected by
0039  C5                  PUSH BC         ; this subroutine.
003A  F5                  PUSH AF         ; Assumed INT mode 1 earlier set.
003B  21 00 3E            LD (HL),X3E00   ; Initialize memory pointer where data will be stored.
003E  0E 01               LD C, X01       ; C register will be port ADDR of A/D converters.
0040  D300                OUT X00, A      ; Load peripheral status word into 8-bit latch.
0042  DB00                IN A, X00       ; Load status word into accumulator.
0044  47                  LD B,A          ; Save the status word.
0045  79          TEST    LD A,C          ; Test to see if the status of all A/D's have
0046  FE 08               CP, X08         ; been checked. If so, exit subroutine
0048  CA 60 00            JPZ, DONE
004B  78                  LD A,B          ; Test a single bit in status word by looking for
004C  1F                  RRA             ; a "1" to be rotated into the CARRY (an INT
004D  47                  LD B,A          ; is loaded as a "1"). If CARRY is set then load
004E  DA 5500             JPC, LOAD       ; contents of A/D at port ADDR in C register.
0051  0C          NEXT    INC C           ; If CARRY is not set, increment C register to point
0052  C3 4500             JP,TEST         ; to next A/D, then test next bit in status word.
0055  ED 78       LOAD    IN A, (C)       ; Read data from interrupting A/D and invert
0057  EE FF               XOR FF          ; the data.
0059  77                  LD (HL),A       ; Store the data
005A  2C                  INC L
005B  71                  LD (HL),C       ; Store A/D identifier (A/D port ADDR).
005C  2C                  INC L
005D  C3 51 00            JP,NEXT         ; Test next bit in status word.
0060  F1          DONE    POP AF          ; Re-establish all registers as they were
0061  C1                  POP BC          ; before the interrupt.
0062  E1                  POP HL
0063  C9                  RET             ; Return to original program
```

DS005671-A6

Physical Dimensions inches (millimeters) unless otherwise noted



SO Package (M)
Order Number ADC0802LCWM or ADC0804LCWM
NS Package Number M20B



Molded Dual-In-Line Package (N)
Order Number ADC0801LCN, ADC0802LCN,
ADC0803LCN, ADC0804LCN or ADC0805LCN
NS Package Number N20A

Notes

LIFE SUPPORT POLICY

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National Semiconductor

February 2000

LM555
Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

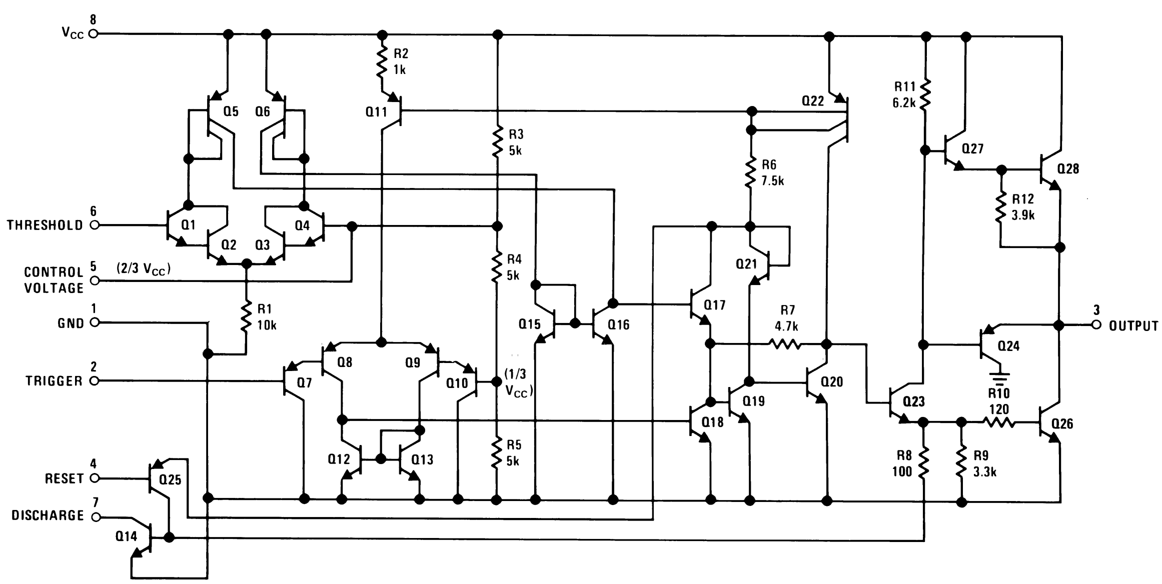
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per ˚C
- Normally on and normally off output
- Available in 8-pin MSOP package

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

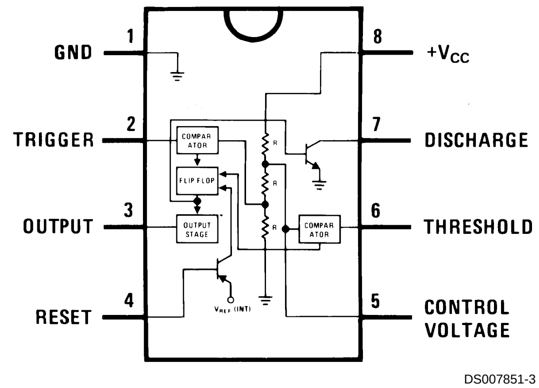
Schematic Diagram



DS007851-1

Connection Diagram

Dual-In-Line, Small Outline and Molded Mini Small Outline Packages



Top View

Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin SOIC	LM555CM	LM555CM	Rails	M08A
	LM555CMX	LM555CM	2.5k Units Tape and Reel	
8-Pin MSOP	LM555CMM	Z55	1k Units Tape and Reel	MUA08A
	LM555CMMX	Z55	3.5k Units Tape and Reel	
8-Pin MDIP	LM555CN	LM555CN	Rails	N08E

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555CM, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C
Soldering Information	
Dual-In-Line Package	
Soldering (10 Seconds)	260˚C
Small Outline Packages (SOIC and MSOP)	
Vapor Phase (60 Seconds)	215˚C
Infrared (15 Seconds)	220˚C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1, 2)

(T_A = 25˚C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Supply Voltage		4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞ (Low State) (Note 4)		3 10	6 15	mA
Timing Error, Monostable					
Initial Accuracy			1		%
Drift with Temperature	R_A = 1k to 100kΩ, C = 0.1µF, (Note 5)		50		ppm/˚C
Accuracy over Temperature			1.5		%
Drift with Supply			0.1		%/V
Timing Error, Astable					
Initial Accuracy			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100kΩ, C = 0.1µF, (Note 5)		150		ppm/˚C
Accuracy over Temperature			3.0		%
Drift with Supply			0.30		%/V
Threshold Voltage			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V V_{CC} = 5V		5 1.67		V V
Trigger Current			0.5	0.9	µA
Reset Voltage		0.4	0.5	1	V
Reset Current			0.1	0.4	mA
Threshold Current	(Note 6)		0.1	0.25	µA
Control Voltage Level	V_{CC} = 15V V_{CC} = 5V	9 2.6	10 3.33	11 4	V
Pin 7 Leakage Output High			1	100	nA
Pin 7 Sat (Note 7)					
Output Low	V_{CC} = 15V, I_7 = 15mA		180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5mA		80	200	mV

Electrical Characteristics (Notes 1, 2) (Continued)

(T_A = 25˚C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V				
	I_{SINK} = 10mA		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.75	V
	I_{SINK} = 100mA		2	2.5	V
	I_{SINK} = 200mA		2.5		V
	V_{CC} = 5V				
	I_{SINK} = 8mA				V
	I_{SINK} = 5mA		0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200mA, V_{CC} = 15V		12.5		V
	I_{SOURCE} = 100mA, V_{CC} = 15V	12.75	13.3		V
	V_{CC} = 5V	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25˚C based on a +150˚C maximum junction temperature and a thermal resistance of 106˚C/W (DIP), 170˚C/W (S0-8), and 204˚C/W (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 5: Tested at V_{CC} = 5V and V_{CC} = 15V.

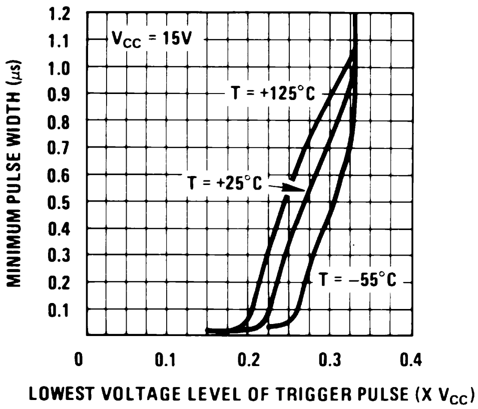
Note 6: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20MΩ.

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 8: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

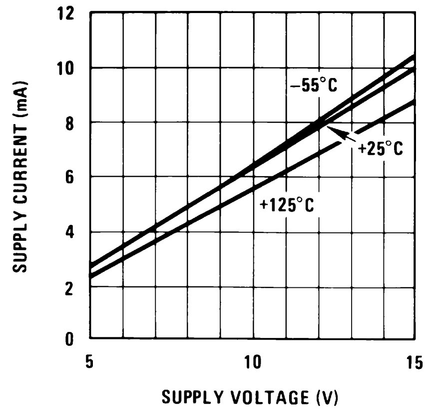
Typical Performance Characteristics

Minimuim Pulse Width Required for Triggering



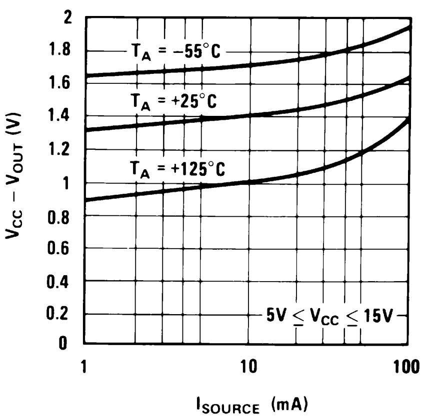
DS007851-4

Supply Current vs. Supply Voltage



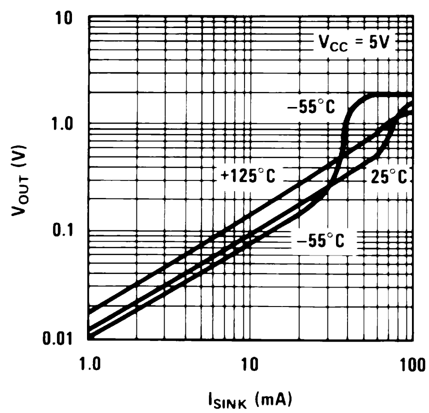
DS007851-19

High Output Voltage vs. Output Source Current



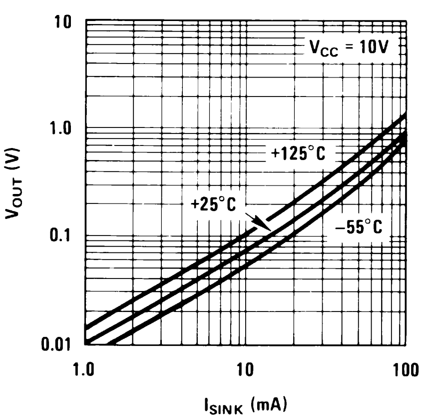
DS007851-20

Low Output Voltage vs. Output Sink Current



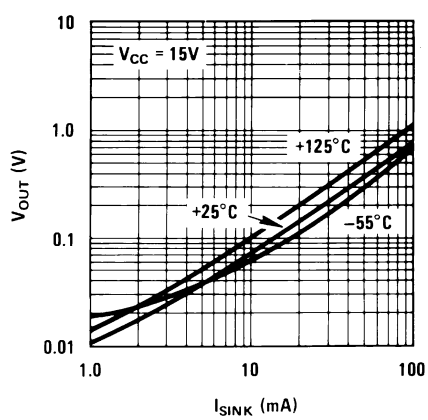
DS007851-21

Low Output Voltage vs. Output Sink Current



DS007851-22

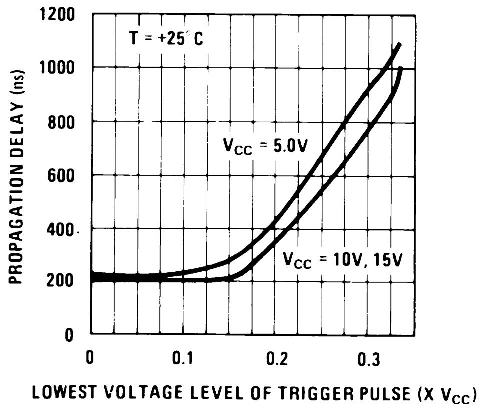
Low Output Voltage vs. Output Sink Current



DS007851-23

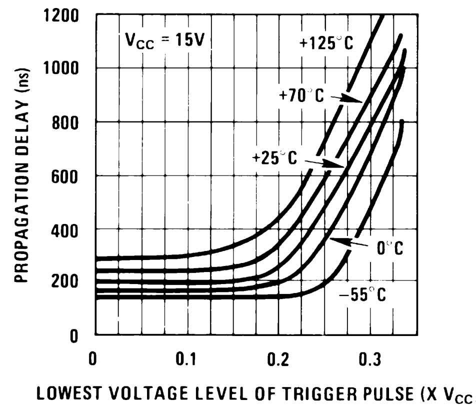
Typical Performance Characteristics (Continued)

Output Propagation Delay vs. Voltage Level of Trigger Pulse



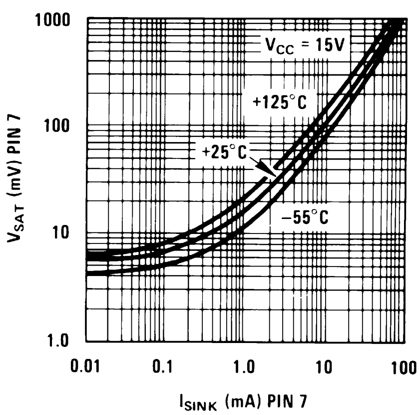
DS007851-24

Output Propagation Delay vs. Voltage Level of Trigger Pulse



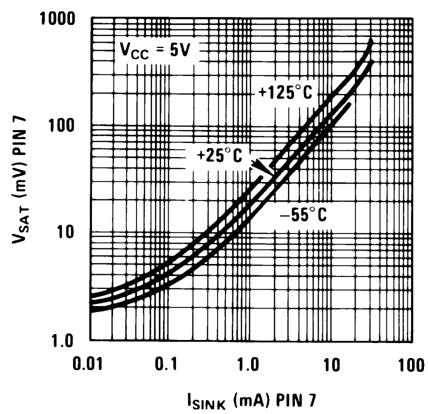
DS007851-25

Discharge Transistor (Pin 7) Voltage vs. Sink Current



DS007851-26

Discharge Transistor (Pin 7) Voltage vs. Sink Current

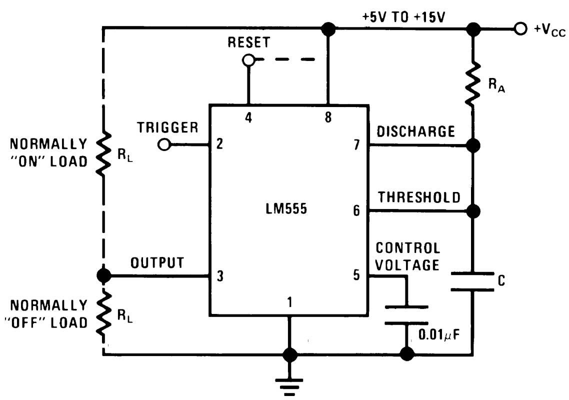


DS007851-27

Applications Information

MONOSTABLE OPERATION

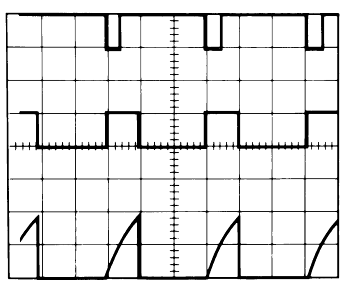
In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.



DS007851-5

FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



DS007851-6

V_{CC} = 5V — Top Trace: Input 5V/Div.
TIME = 0.1 ms/DIV. — Middle Trace: Output 5V/Div.
R_A = 9.1kΩ — Bottom Trace: Capacitor Voltage 2V/Div.
C = 0.01µF

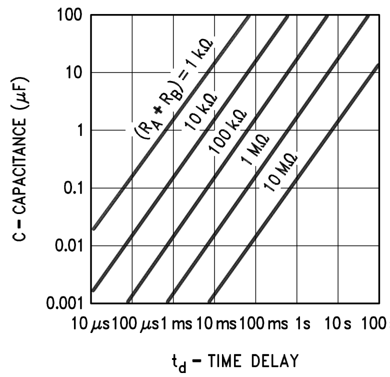
FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10µs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

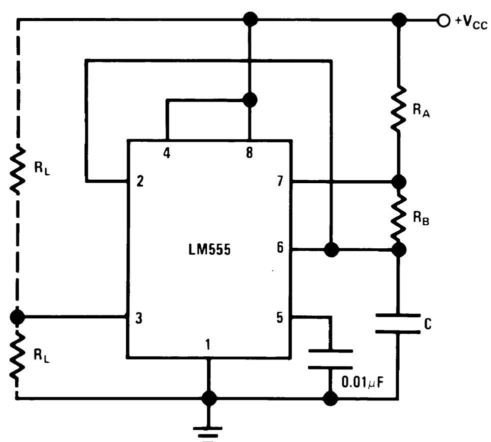


DS007851-7

FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.



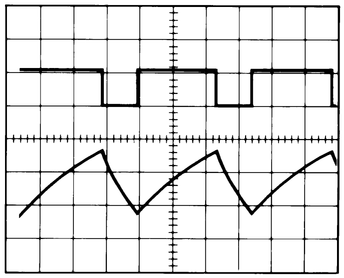
DS007851-8

FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



V_{CC} = 5V Top Trace: Output 5V/Div.
TIME = 20µs/DIV. Bottom Trace: Capacitor Voltage 1V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2\,R_B)\,C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

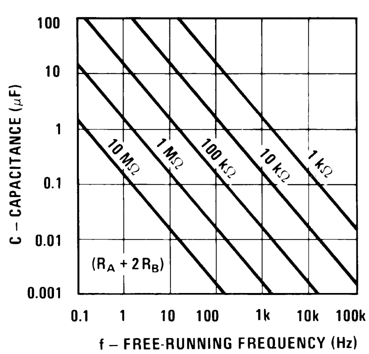
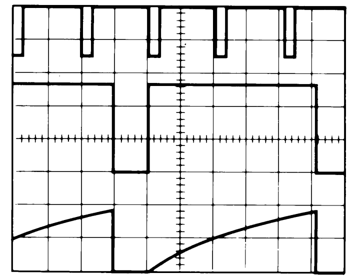


FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



V_{CC} = 5V Top Trace: Input 4V/Div.
TIME = 20µs/DIV. Middle Trace: Output 2V/Div.
R_A = 9.1kΩ Bottom Trace: Capacitor 2V/Div.
C = 0.01µF

FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

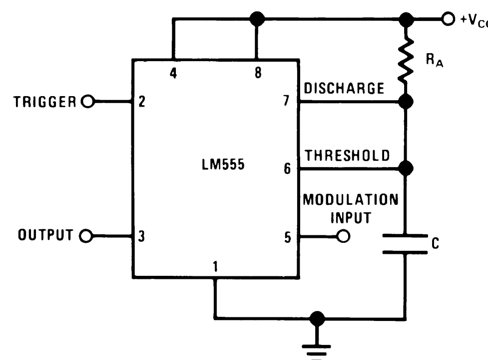
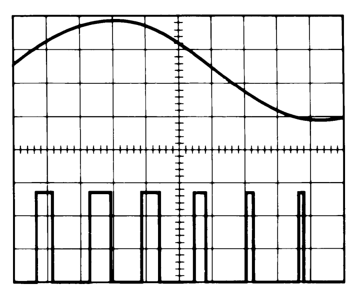


FIGURE 8. Pulse Width Modulator



V_{CC} = 5V Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV. Bottom Trace: Output Voltage 2V/Div.
R_A = 9.1kΩ
C = 0.01µF

FIGURE 9. Pulse Width Modulator

Applications Information (Continued)

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

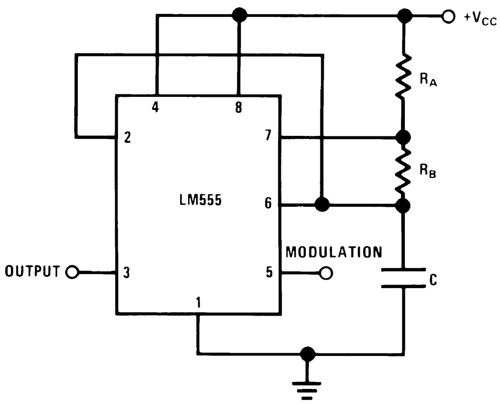
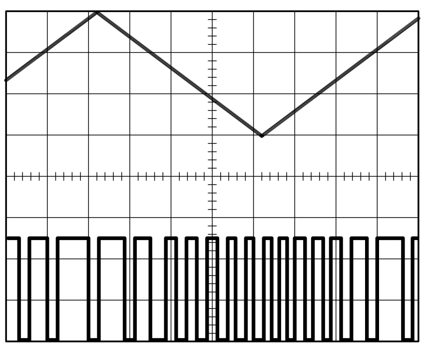


FIGURE 10. Pulse Position Modulator



V_{CC} = 5V   Top Trace: Modulation Input 1V/Div.
TIME = 0.1 ms/DIV.   Bottom Trace: Output 2V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.

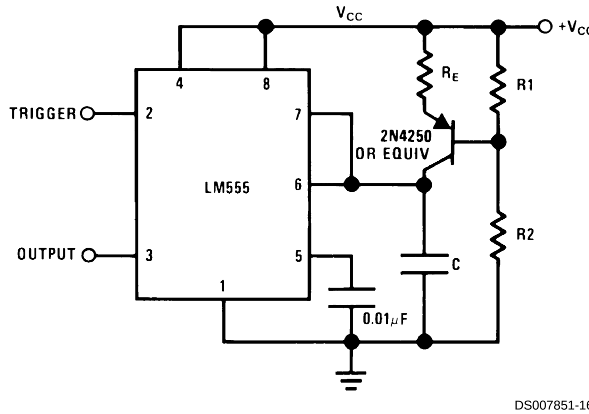


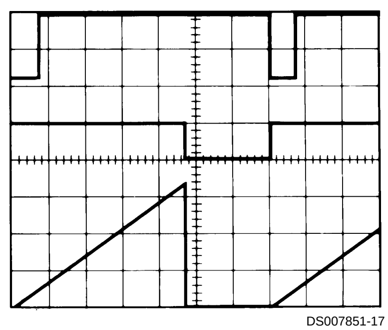
FIGURE 12.

Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3\, V_{CC}\, R_E\, (R_1 + R_2)\, C}{R_1\, V_{CC} - V_{BE}\, (R_1 + R_2)}$$

$$V_{BE} \cong 0.6V$$

$$V_{BE} \simeq 0.6V$$



V_{CC} = 5V   Top Trace: Input 3V/Div.
TIME = 20µs/DIV.   Middle Trace: Output 5V/Div.
R_1 = 47kΩ   Bottom Trace: Capacitor Voltage 1V/Div.
R_2 = 100kΩ
R_E = 2.7 kΩ
C = 0.01 µF

FIGURE 13. Linear Ramp

Applications Information (Continued)

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is t_2 =

$$\left[(R_A R_B)/(R_A + R_B)\right] C\ \ell n \left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$

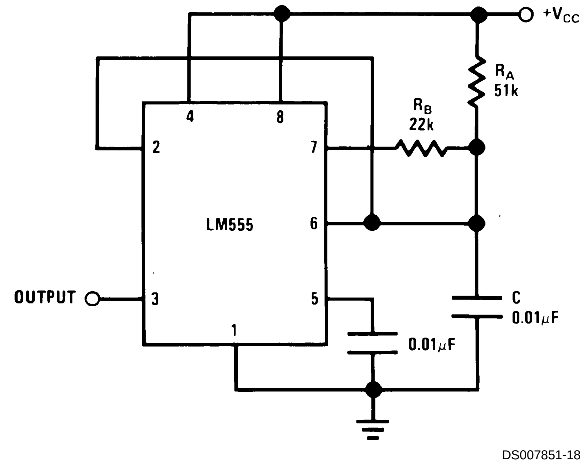


FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

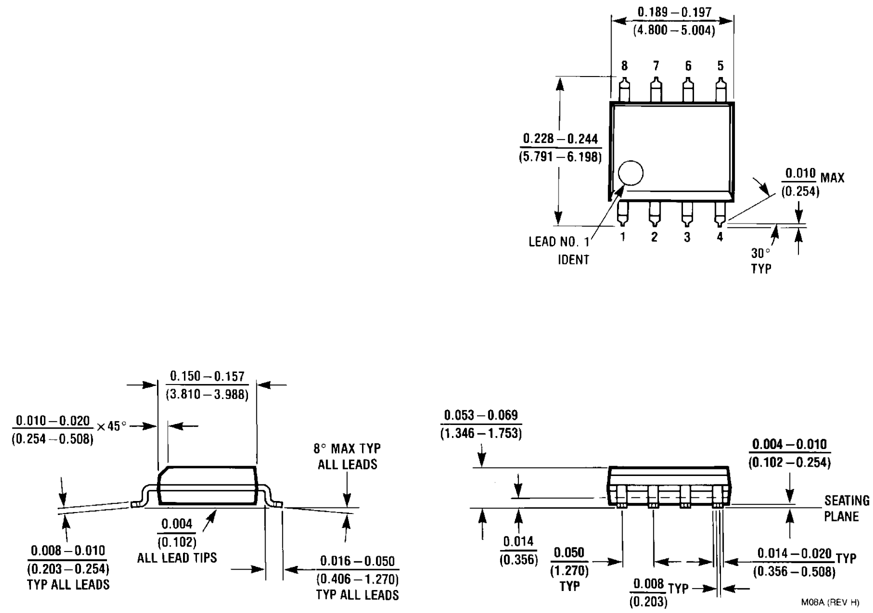
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

Lower comparator storage time can be as long as 10µs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10µs minimum.

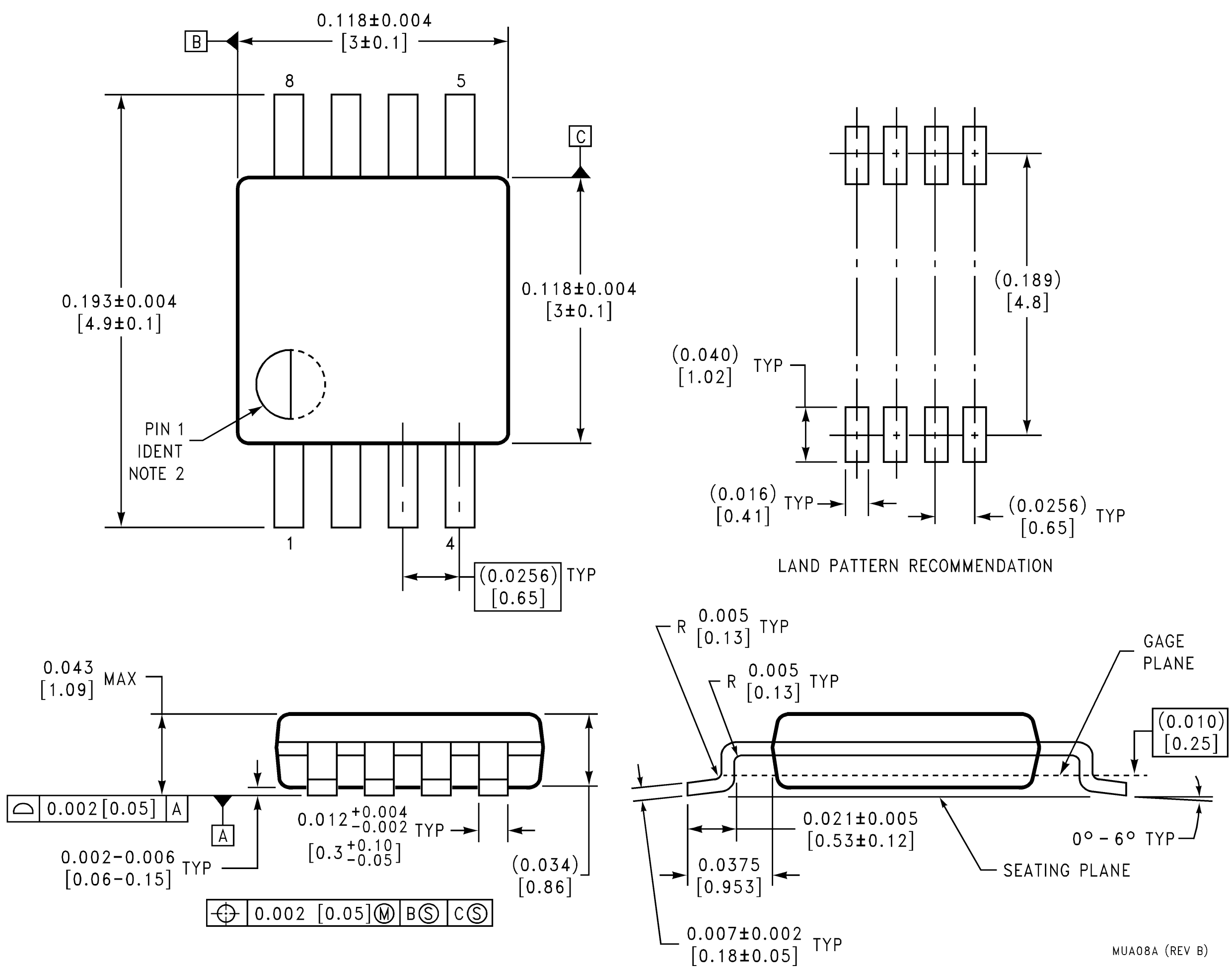
Delay time reset to output is 0.47µs typical. Minimum reset pulse width must be 0.3µs, typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

Physical Dimensions inches (millimeters) unless otherwise noted

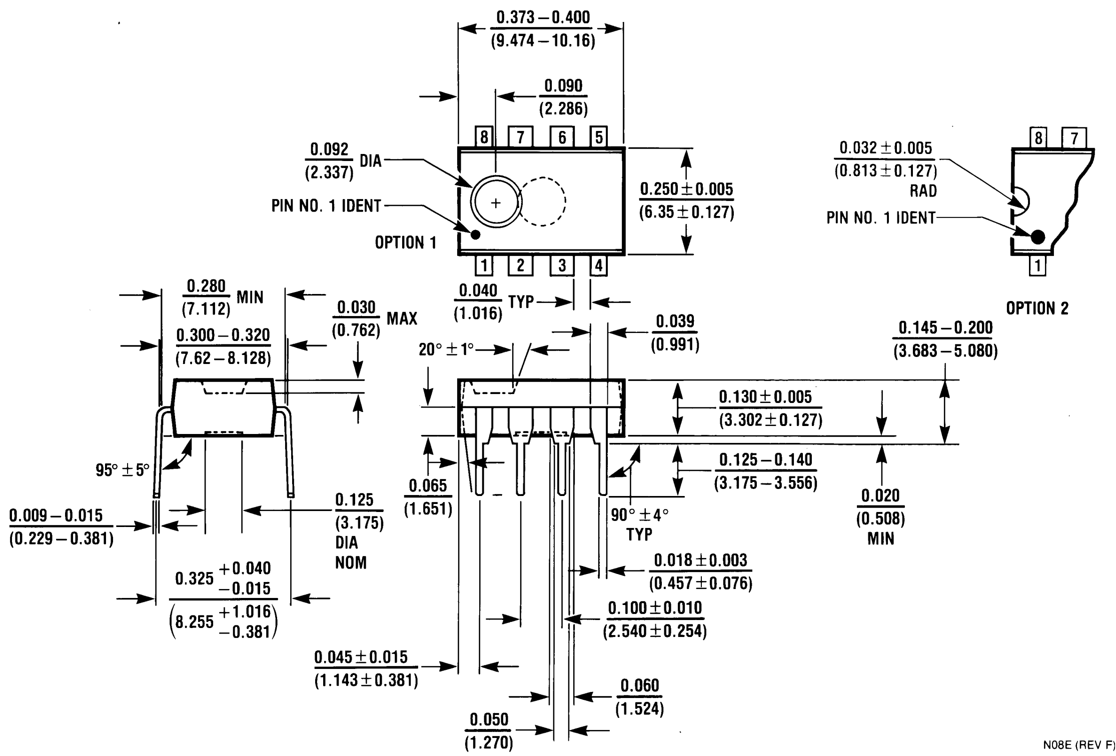


Small Outline Package (M)
NS Package Number M08A



8-Lead (0.118” Wide) Molded Mini Small Outline Package
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
NS Package Number N08E

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

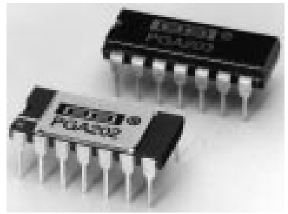
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BURR - BROWN ®



PGA202/203

Digitally Controlled Programmable-Gain INSTRUMENTATION AMPLIFIER

FEATURES

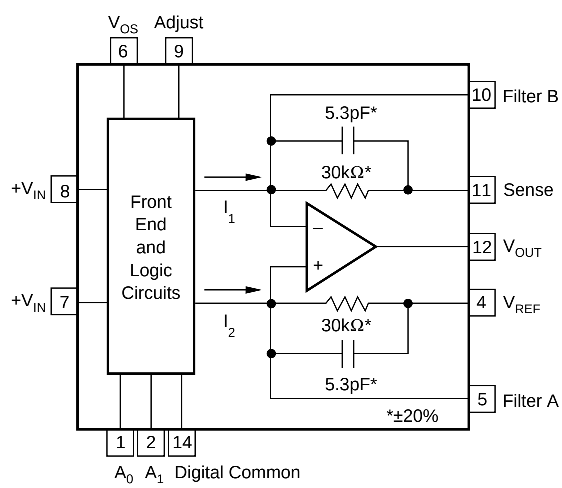
- DIGITALLY PROGRAMMABLE GAINS:
  DECADE MODEL—PGA202
  GAINS OF 1, 10, 100, 1000
  BINARY MODEL—PGA203
  GAINS OF 1, 2, 4, 8
- LOW BIAS CURRENT: 50pA max
- FAST SETTLING: 2µs to 0.01%
- LOW NON-LINEARITY: 0.012% max
- HIGH CMRR: 80dB min
- NEW TRANSCONDUCTANCE CIRCUITRY
- LOW COST

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- AUTO-RANGING CIRCUITS
- DYNAMIC RANGE EXPANSION
- REMOTE INSTRUMENTATION
- TEST EQUIPMENT

DESCRIPTION

The PGA202 is a monolithic instrumentation amplifier with digitally controlled gains of 1, 10, 100, and 1000. The PGA203 provides gains of 1, 2, 4, and 8. Both have TTL or CMOS-compatible inputs for easy microprocessor interface. Both have FET inputs and a new transconductance circuitry that keeps the bandwidth nearly constant with gain. Gain and offsets are laser trimmed to allow use without any external components. Both amplifiers are available in ceramic or plastic packages. The ceramic package is specified over the full industrial temperature range while the plastic package covers the commercial range.



Covered by U.S. PATENT #4,883,422

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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

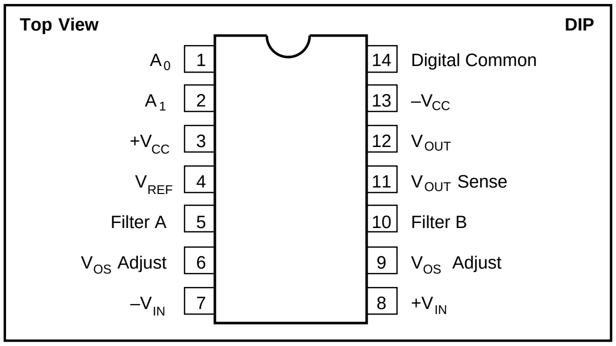
At +25°C, V_{CC} = ±15V unless otherwise noted.

PARAMETER	CONDITION	PGA202/203AG (1)			PGA202/203BG (1)			PGA202/203KP (1)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Error (2)	G < 1000		0.05	0.25		*	0.15		*	*	%
	G = 1000		0.1	1		0.08	0.5		*	*	%
Nonlinearity	G < 1000		0.002	0.015		*	0.012		*	*	%
	G = 1000		0.02	0.06		*	0.04		*	*	%
Gain vs Temperature	G < 100		3	25		*	15		*		ppm/°C
	G = 100		40	120		*	60		*		ppm/°C
	G = 1000		100	300		*	150		*		ppm/°C
RATED OUTPUT											
Voltage	$\lvert I_{OUT} \rvert \leq$ 5mA	±10	±12		*	*		*	*		V
Over Specified Temperature	See Typical Perf. Curve		±9			*			±10		V
Current	$\lvert V_{OUT} \rvert \leq$ 10V	±5	±10		*	*		*	*		mA
Impedance			0.5			*			*		Ω
ANALOG INPUTS											
Common-Mode Range		±10	±13		*	*		*	*		V
Absolute Max Voltage (3)	No Damage			$\pm V_{CC}$			*			*	V
Impedance, Differential			10 || 3			*			*		GΩ || pF
Common-Mode			10 || 1			*			*		GΩ || pF
OFFSET VOLTAGE (RTI)											
Initial Offset at 25°C (4)			±(0.5 + 5/G)	±(2 + 24/G)		*	±(1 + 12/G)		*	*	mV
vs Temperature			±(3 + 50/G)	±(24 + 240/G)		*	±(12 + 120/G)		*		µV/°C
Offset vs Time			50			*			*		µV/Month
Offset vs Supply	$10 \leq V_{CC} \leq 15$		10 + 250/G	100 + 900/G		*	50 + 450/G		*	*	µV/V
INPUT BIAS CURRENT											
Initial Bias Current: at 25°C			10	50		*	*		*	*	pA
at 85°C			640	3200		*	*		*	*	pA
Initial Offset Current: at 25°C			5	25		*	*		*	*	pA
at 85°C			320	1600		*	*		*	*	pA
COMMON-MODE REJECTION RATIO											
	G = 1	80	100		*	*		*	*		dB
	G = 10	86	110		*	*		*	*		dB
	G = 100	92	120		*	*		*	*		dB
	G = 1000	94	120		*	*		*	*		dB
INPUT NOISE											
Noise Voltage 0.1 to 10Hz			1.7			*			*		µVp-p
Noise Density at 10kHz (5)			12			*			*		nV/√Hz
OUTPUT NOISE											
Noise Voltage 0.1 to 10Hz			32			*			*		µVp-p
Density at 1kHz (5)			400			*			*		nV/√Hz
DYNAMIC RESPONSE											
Frequency Response	G < 1000		1000			*			*		kHz
	G = 1000		250			*			*		kHz
Full Power Bandwidth	G < 1000		400			*			*		kHz
	G = 1000		100			*			*		kHz
Slew Rate		10	20		15	*		*	*		V/µs
Settling Time (0.01%) (7)	G < 1000		2			*			*		µs
	G = 1000		10			*			*		µs
Overload Recovery Time (7)	G < 1000		5			*			*		µs
	G = 1000		10			*			*		µs
DIGITAL INPUTS											
Digital Common Range		$-V_{CC}$		$V_{CC} - 8$	*		*	*		*	V
Input Low Threshold (6)				0.8			*			*	V
Input Low Current				10			*			*	µA
Input High Voltage		2.4			*			*			V
Input High Current				10			*			*	µA
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range		±6		±18	*		*	*		*	V
Quiescent Current			6.5			*			*		mA
TEMPERATURE RANGE											
Specification		–25		85	*		*	0		70	°C
Operating		–55		125	*		*	–25		85	°C
Storage		–65		150	*		*	–40		100	°C
θ_{JA}			100			*			*		°C/W

* Same as the PGA202/203AG

NOTES: (1) All specifications apply to both the PGA202 and the PGA203. Values given for a gain of 10 are the same for a gain of 8 and other values may be interpolated. (2) Measured with a 10k load. (3) The analog inputs are internally diode clamped. (4) Adjustable to zero. (5) $V_{NOISE\ (RTI)} = \sqrt{(V_{N\ INPUT})^2 + (V_{N\ OUTPUT}/Gain)^2}$. (6) Threshold voltages are referenced to Digital Common. (7) From input change or gain change.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation	750mW
Analog and Digital Inputs	$\pm(V_{CC} + 0.5V)$
Operating Temperature Range:	
G Package	–55°C to +125°C
P Package	–40°C to +100°C
Lead Temperature (soldering, 10s)	300°C
Output Short Circuit Duration	Continuous
Junction Temperature	175°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
PGA202KP	14-Pin Plastic DIP	010
PGA202AG	14-Pin Ceramic DIP	169
PGA202BG	14-Pin Ceramic DIP	169
PGA203KP	14-Pin Plastic DIP	010
PGA203AG	14-Pin Ceramic DIP	169
PGA203BG	14-Pin Ceramic DIP	169

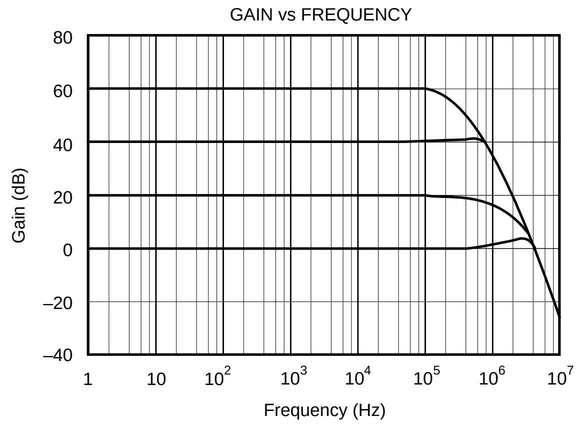
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

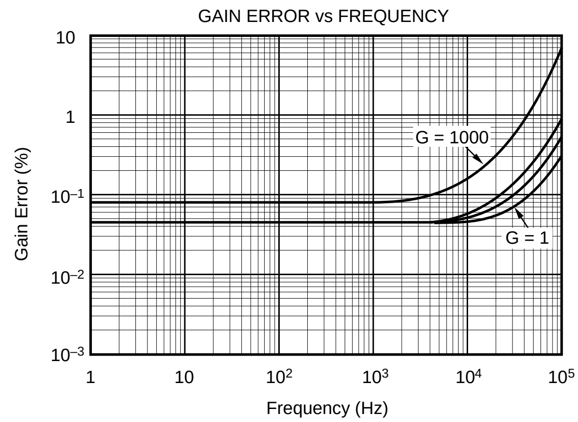
ORDERING INFORMATION

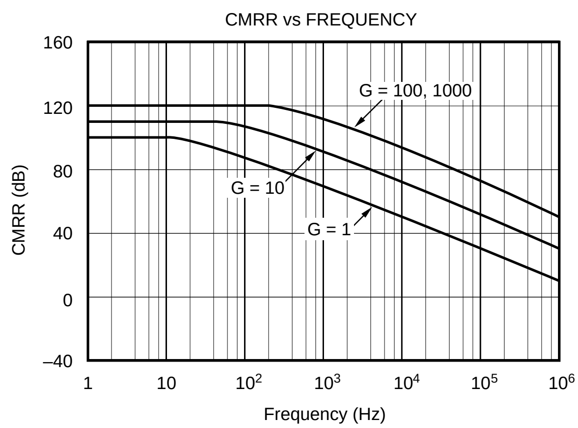
MODEL	GAINS	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE MAX (mV)
PGA202KP	1, 10, 100, 1000	Plastic DIP	0°C to +70°C	±(2 + 24/G)
PGA202AG	1, 10, 100, 1000	Ceramic DIP	–25°C to +85°C	±(2 + 24/G)
PGA202BG	1, 10, 100, 1000	Ceramic DIP	–25°C to +85°C	±(1 + 12/G)
PGA203KP	1, 2, 4, 8	Plastic DIP	0°C to +70°C	±(2 + 24/G)
PGA203AG	1, 2, 4, 8	Ceramic DIP	–25°C to +85°C	±(2 + 24/G)
PGA203BG	1, 2, 4, 8	Ceramic DIP	–25°C to +85°C	±(1 + 12/G)

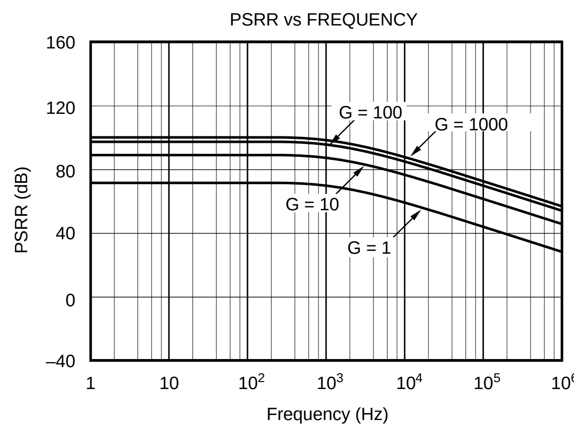
TYPICAL PERFORMANCE CURVES

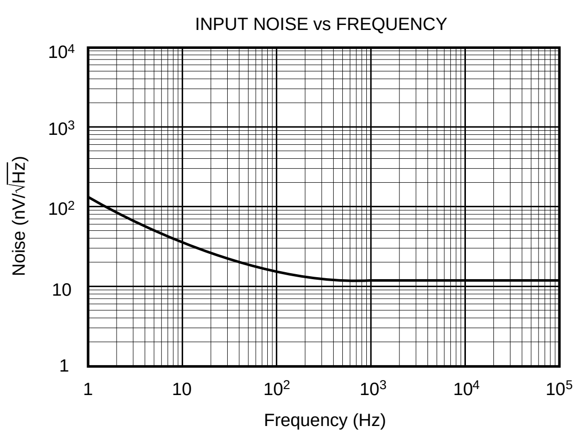
T_A = +25°C, V_S = ±15V unless otherwise noted.

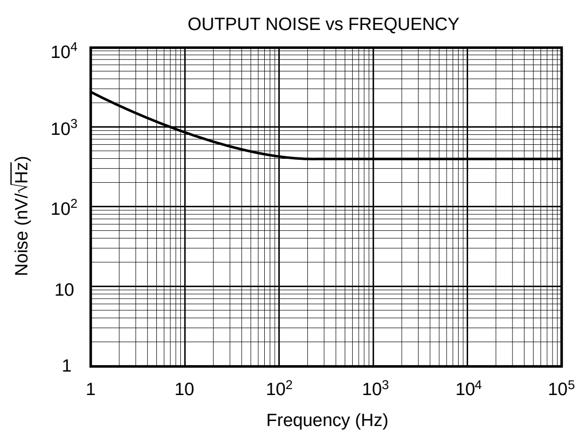






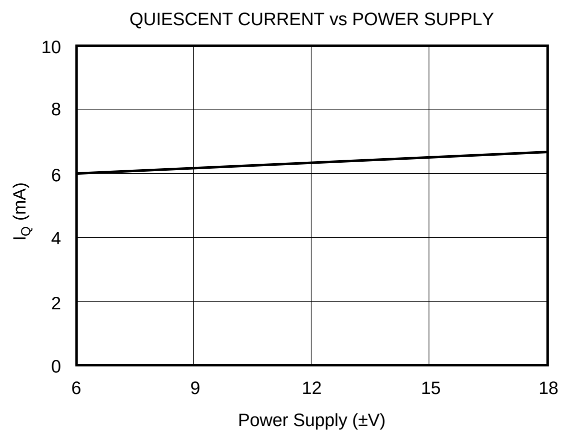


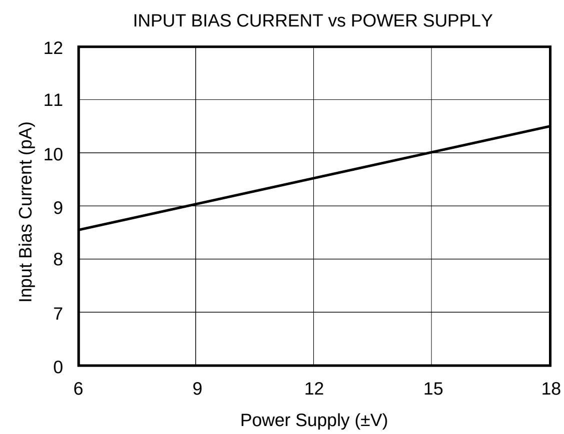


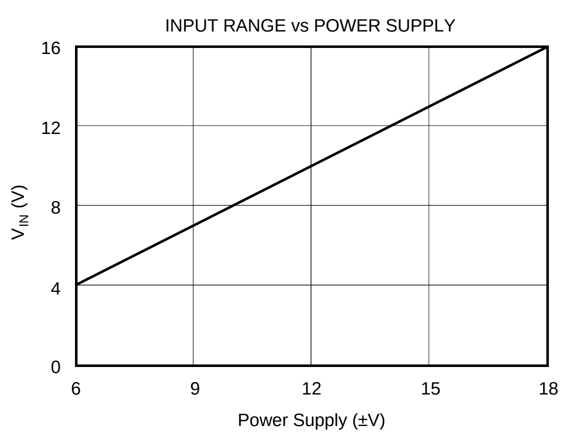


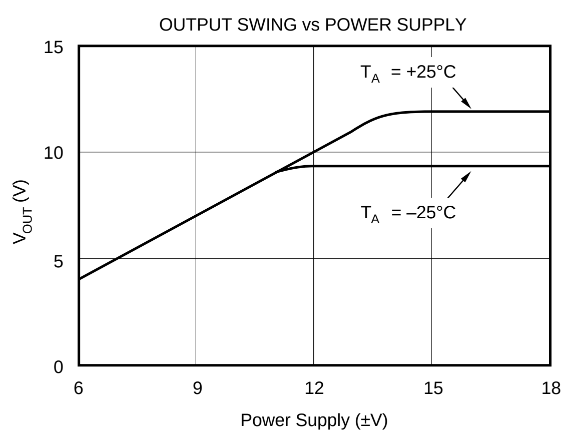
TYPICAL PERFORMANCE CURVES (CONT)

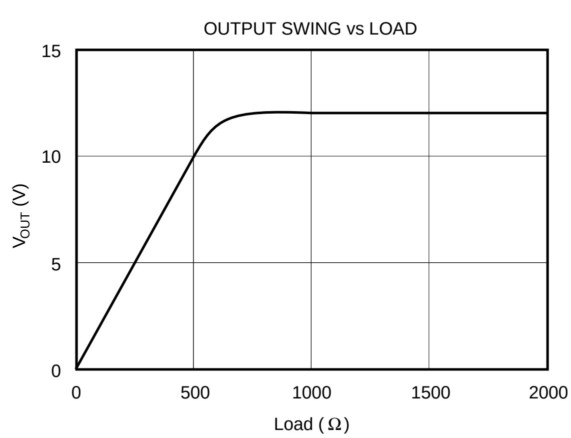
$T_A = +25°C$, $V_S = ±15V$ unless otherwise noted.

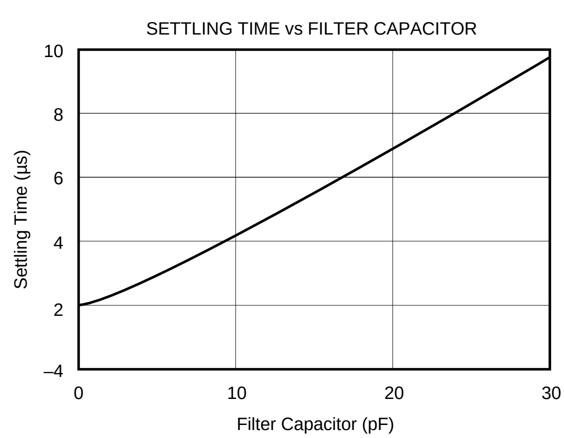






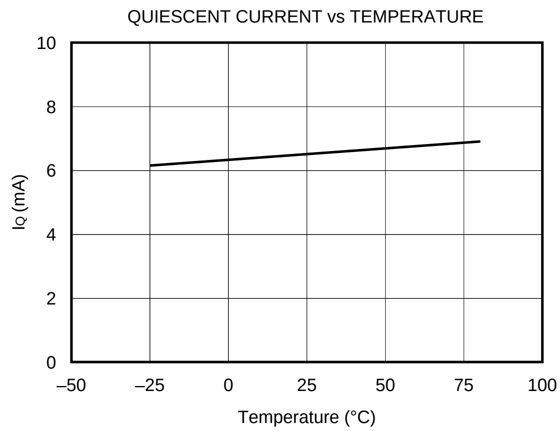


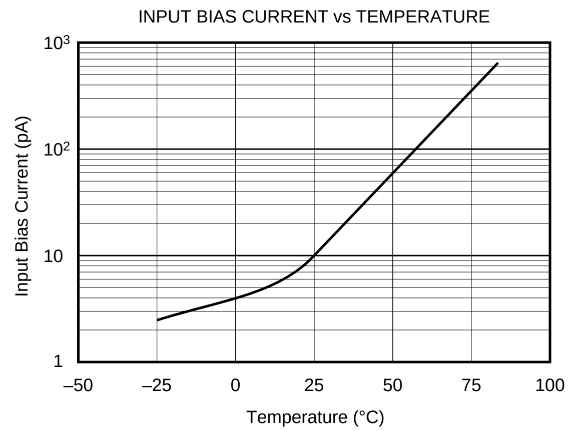


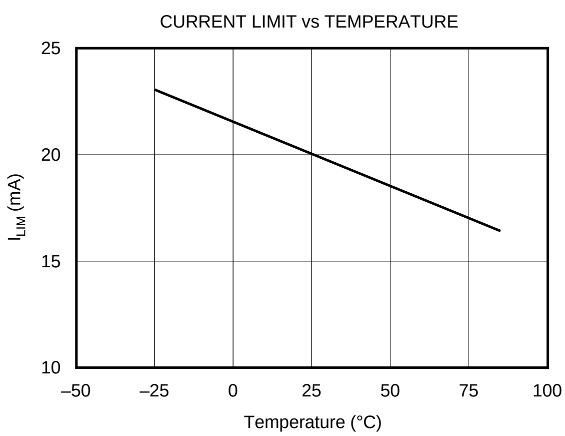


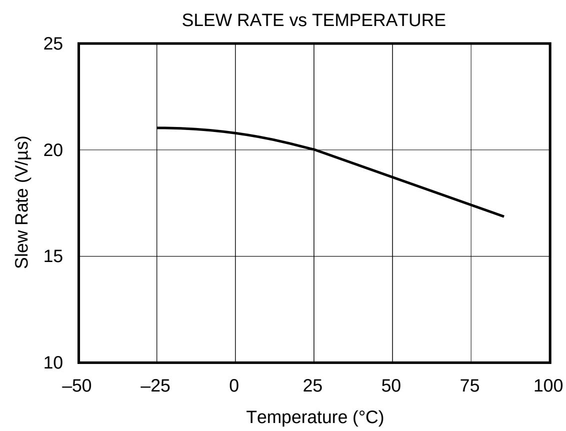
TYPICAL PERFORMANCE CURVES (CONT)

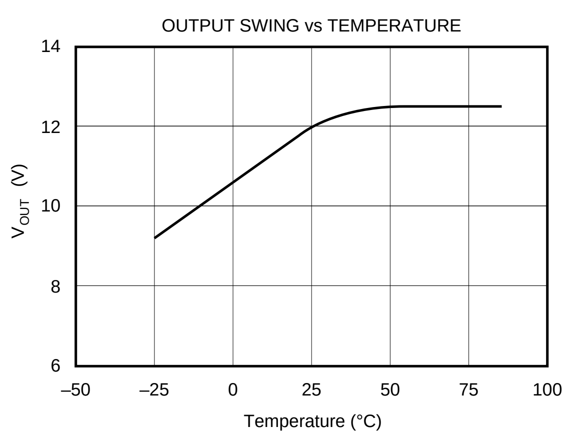
T_A = +25°C, V_S = ±15V unless otherwise noted.

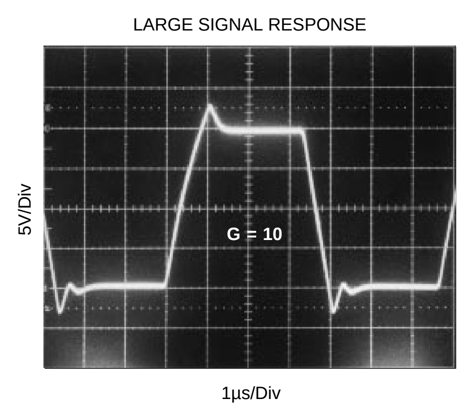






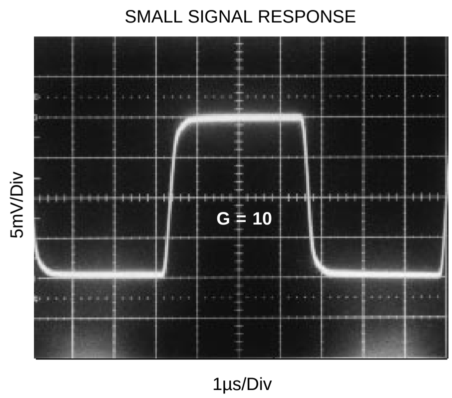






TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.



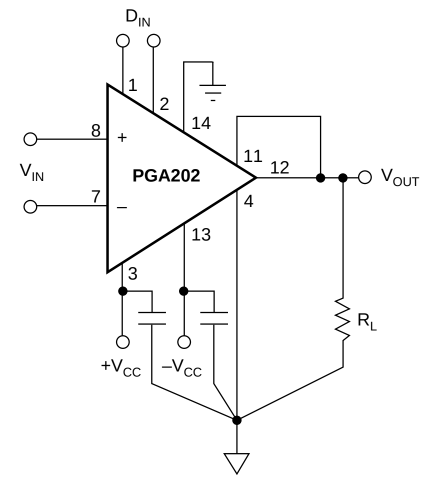


FIGURE 1. Basic Circuit Connections.

DISCUSSION OF PERFORMANCE

A simplified diagram of the PGA202/203 is shown on the first page. The design consists of a digitally controlled, differential transconductance front end stage using precision FET buffers and the classical transimpedance output stage. Gain switching is accomplished with a novel current steering technique that allows for fast settling when changing gains. The result is a high performance, programmable instrumentation amplifier with excellent speed and gain accuracy.

The input stage uses a new circuit topology that includes FET buffers to give extremely low input bias currents. The differential input voltage is converted into a differential output current with the transconductance gain selected by steering the input stage bias current between four identical input stages differing only in the value of the gain setting resistor. Each input stage is individually laser-trimmed for input offset, offset drift, and gain.

The output stage is a differential transimpedance amplifier. Unlike the classical difference amplifier output stage, the common-mode rejection is not limited by the resistor matching. However, the output resistors are laser-trimmed to help minimize the output offset and drift.

BASIC CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. The power supplies should be decoupled with 1µF tantalum capacitors placed as close to the amplifier as possible for maximum performance. To avoid gain and CMR errors introduced by the external components, you should connect the grounds as indicated. Any resistance in the sense line (pin 11) or the V_{REF} line (pin 4) will lead to a gain error, so these lines should be kept as short as possible. To also maintain stability, avoid capacitance from the output to the input or the offset adjust pins.

OFFSET ADJUSTMENT

Figure 2 shows the offset adjustment circuits for the PGA202/203. The input offset and the output offset are both separately adjustable. Notice that because the PGA202/203 change between four different input stages to change gain, the input offset voltage will change slightly with gain. For systems using computer autozeroing techniques, neither offset nor drift is a major concern, but it should be noted that since the input offset does change with gain, these systems should perform an autozero cycle after each gain change for optimum performance.

In the output offset adjustment circuit, the choice of the buffering op amp is very important. The op amp needs to have low output impedance and a wide bandwidth to maintain full accuracy over the entire frequency range of the PGA202/203. For these reasons we recommend the OPA602 as an excellent choice for this application.

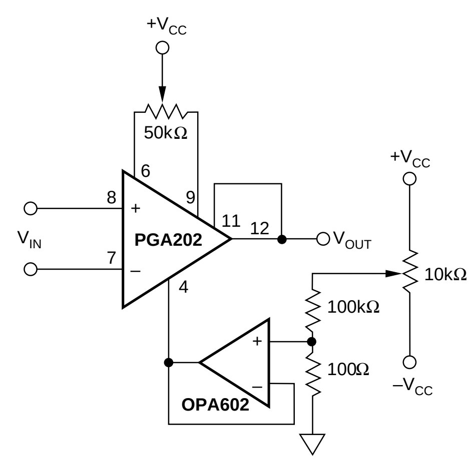


FIGURE 2. Offset Adjustment Circuits.

GAIN SELECTION

Gain selection is accomplished by the application of a 2-bit digital word to the gain select inputs. Table I shows the gains for the different possible values of the digital input word. The logic inputs are referred to their own separate digital common pin, which can be connected to any voltage between the minus supply and 8V below the positive supply. The gains are all internally trimmed to an initial accuracy of better than 0.1%, so no external gain adjustment is required. However, if necessary the gains can be increased by the use of an external attenuator around the output stage as shown in Figure 3. Recommended resistor values for certain selected output gains are given in Table II.

		PGA202		PGA203	
A_1	A_0	GAIN	ERROR	GAIN	ERROR
0	0	1	0.05%	1	0.05%
0	1	10	0.05%	2	0.05%
1	0	100	0.05%	4	0.05%
1	1	1000	0.10%	8	0.05%

TABLE I. Software Gain Selection.

OUTPUT GAIN	R_1	R_2
2	5kΩ	5kΩ
5	2kΩ	8kΩ
10	1kΩ	9kΩ

TABLE II. Output Stage Gain Control.

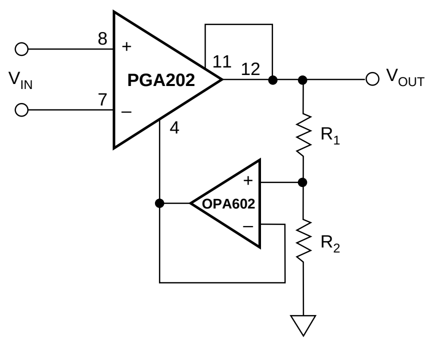


FIGURE 3. Gain Increase with Buffered Attenuator.

COMMON-MODE INPUT RANGE

Unlike the classical three op amp type of circuit, the input common-mode range of the PGA202/203 does not depend on the differential input and the gain. In the standard three op amp circuit, the input common-mode signal must be kept below the maximum output voltage of the input amplifier minus 1/2 the final output voltage. If, for example, these amplifiers can swing ±12V, then to get 12V at the output you must restrict the input common-mode voltage to only 6V. The circuitry of the PGA202/203 is such that the common-mode input range applies to either input pin regardless of the output voltage.

OUTPUT SENSE

An output sense has been provided to allow greater accuracy in connecting the load. By attaching this feedback point to the load at the load site, IR drops due to the load currents are eliminated since they are inside the feedback loop. Proper connection is shown in Figure 1. When more current is required, a power booster can be placed in the feedback loop as shown in Figure 4. Buffer errors are minimized by the loop gain of the output amplifier.

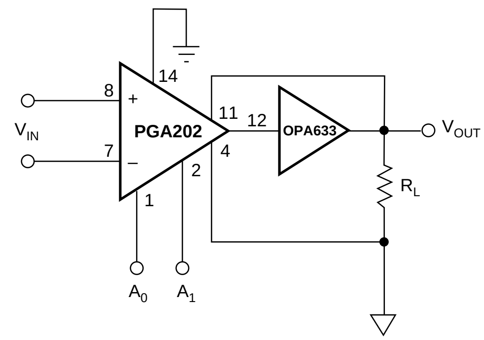


FIGURE 4. Current Boosting the Output.

OUTPUT FILTERING

The summing nodes of the output amplifier have also been made available to allow for output filtering. By placing matched capacitors in parallel with the existing internal capacitors as shown in Figure 5, you can lower the frequency response of the output amplifier. This will reduce the noise of the amplifier, at the cost of a slower response. The nominal frequency responses for some selected values of capacitor are shown in Table III.

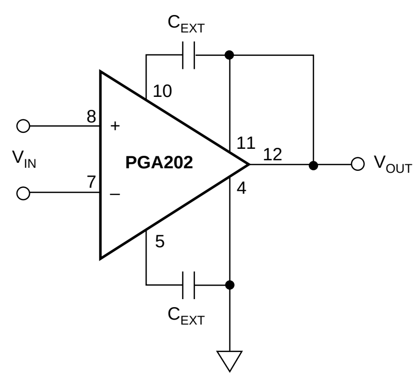


FIGURE 5. Output Filtering.

CUTOFF FREQUENCY	C_1 AND C_2
1MHz	None
100kHz	47pF
10kHz	525pF

TABLE III. Output Frequency vs Filter Capacitors.

INPUT CHARACTERISTICS

Because the PGA202/203 have FET inputs, the bias currents drawn through input source resistors have a negligible effect on DC accuracy. The picoamp currents produce no more than microvolts through megohm sources. The inputs are also internally diode clamped to the supplies. Thus, input filtering and input series protection are easily achievable.

A return path for the input bias currents must always be provided to prevent the charging of any stray capacitance. Otherwise, the amplifier could wander and saturate. A 1MΩ to 10MΩ resistor from the input to common will return floating sources such as thermocouples and AC-coupled inputs (see Applications Section, Figures 8 and 9.)

DYNAMIC PERFORMANCE

The PGA202 and the PGA203 are fast-settling FET input programmable gain instrumentation amplifiers. Careful attention to minimize stray capacitance is necessary to achieve specified performance. High source resistance will interact with the input capacitance to reduce speed and overall bandwidth. Also, to maintain stability, avoid capacitance from the output to the input or the offset adjust pins.

Applications with balanced source impedance will provide the best performance. In some applications, mismatched source impedances may be required. If the impedance in the negative input exceeds that in the positive input, stray capacitance from the output will create a net negative feedback and improve the stability of the circuit. If, however, the impedance in the positive input is greater, then the feedback due to stray capacitance will be positive and instability may result. The degree of positive feedback will, of course, depend on the source impedance imbalance as well as the board layout and the operating gain. The addition of a small bypass capacitor of about 5 to 50pF directly across the input terminals of the PGIA will generally eliminate any instability arising from these stray capacitances. CMR errors due to the source imbalance will also be reduced by the addition of this capacitor.

The PGA202 and the PGA203 are designed for fast settling in response to changes in either the input voltage or the gain. The bandwidth and the settling times are mostly determined by the output stage and are therefore independent of gain, except at the highest gain of the PGA202 where other factors in the input stage begin to dominate.

APPLICATIONS

In addition to general purpose applications, the PGA202/203 are designed to handle two important and demanding classes of applications: inputs with high source impedances, and rapid scanning data acquisition systems requiring fast settling time. Because the user has access to output sense and output common pins, current sources can also be constructed with a minimum of external components. Some basic application circuits are shown in Figures 6 through 12.

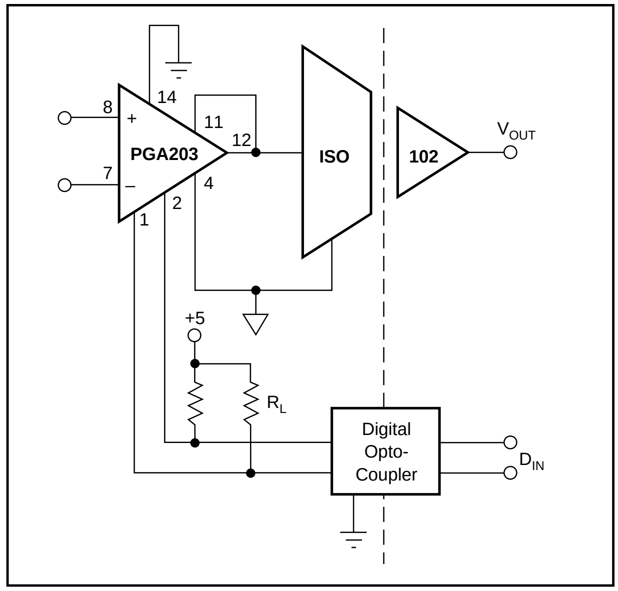


FIGURE 6. Isolated Programmable Gain Instrumentation Amplifier.

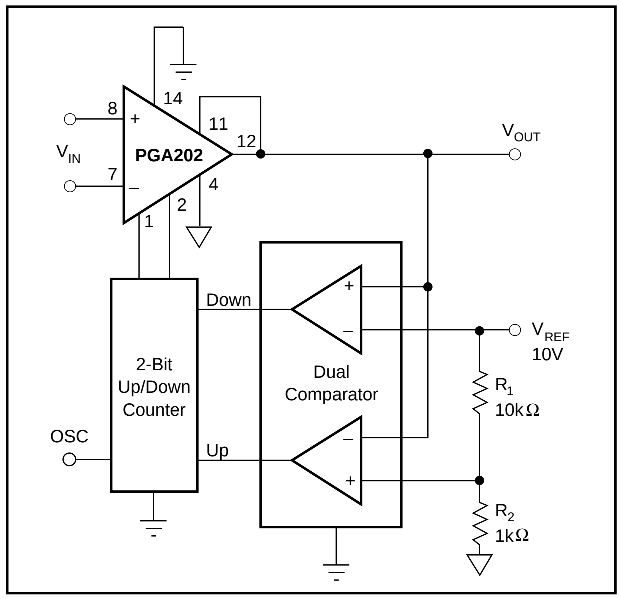


FIGURE 7. Auto Gain Ranging.

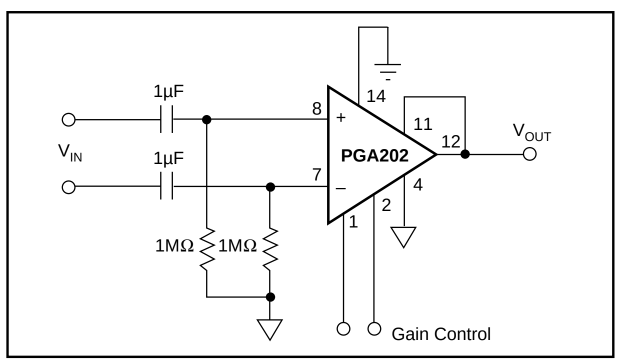


FIGURE 8. AC-Coupled Differential Amplifier for Frequencies Above 0.16Hz.

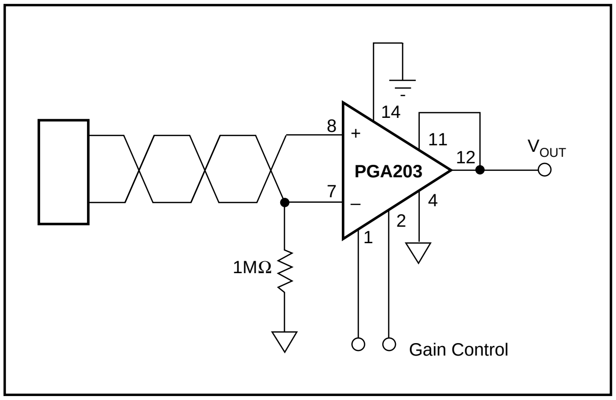


FIGURE 9. Floating Source Programmable Gain Instrumentation Amplifier.

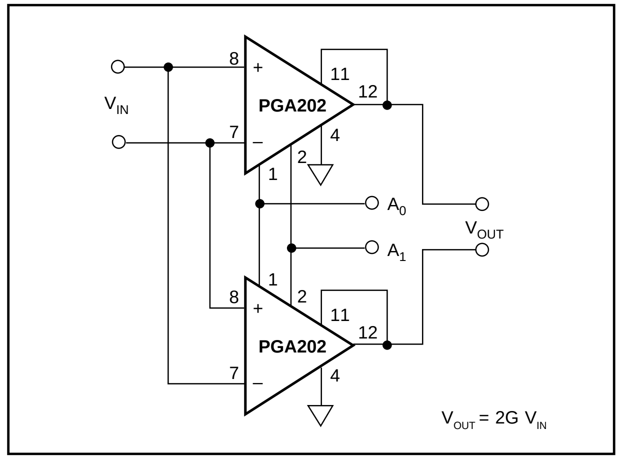


FIGURE 11. Programmable Differential In/Differential Out Amplifier.

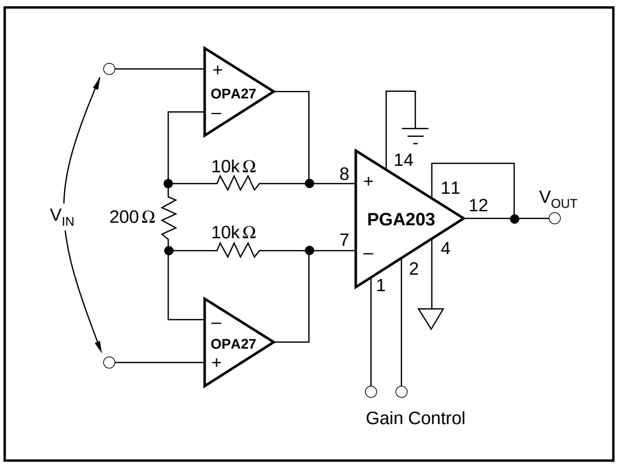


FIGURE 10. Low Noise Differential Amplifier with Gains of 100, 200, 400, 800.

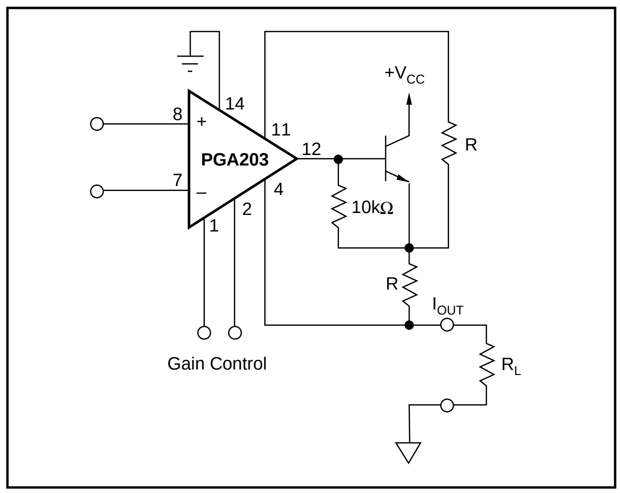
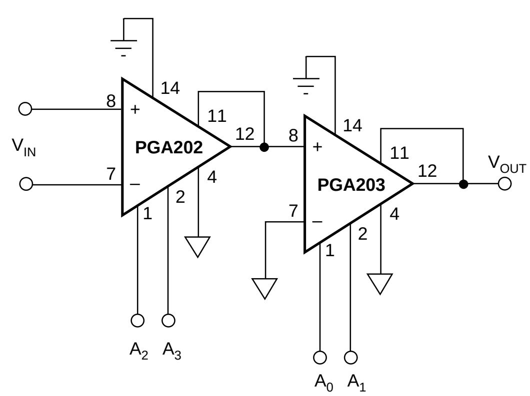


FIGURE 12. Programmable Current Source.



A_3	A_2	A_1	A_0	GAIN
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	8
0	1	0	0	10
0	1	0	1	20
0	1	1	0	40
0	1	1	1	80
1	0	0	0	100
1	0	0	1	200
1	0	1	0	400
1	0	1	1	800
1	1	0	0	1000
1	1	0	1	2000
1	1	1	0	4000
1	1	1	1	8000

FIGURE 13. Cascaded Amplifiers.